MODELING AND SIMULATION OF THE FULLY DEPLETED SILICON-ON-INSULATOR MOSFET FOR SUBMICRON CMOS IC DESIGN

By

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This dissertation concerns physical modeling and simulation of the fully depleted silicon-on-insulator (SOI) MOS field-effect transistor (MOSFET) for submicron complementary-MOS (CMOS) integrated circuit (IC) design. Design issues are studied, focusing on the hot-carrier-related device degradation and the floating-body effects, which are the main concerns regarding the contemporary scaled technology. The hot-carrier-related device degradation is monitored by the impact-ionization current in the MOSFET, and a moderate (not ultra-thin) SOI film thickness is suggested to reduce the high drain field that underlies the degradation. Floating-body effects, which are difficult to characterize by measurements, are intensively analyzed through numerical device simulations. The off-state latch

resulting from activation of the parasitic bipolar junction transistor (BJT) is found to be most detrimental to circuit performance, and a lightly doped source (LDS) structure is suggested to limit the BJT current gain and suppress the latch. A new model for the fully depleted SOI MOSFET that accounts for the important features, including the subthreshold conduction, the parasitic BJT effects, the effects of the LDS and the lightly doped drain (LDD), and the thermal generation current, is developed. The model is physical, requiring semi-numerical analyses, and therefore is applicable to devices having any channel length for any SOI film thickness, so long as the full-depletion assumption is valid. The model is implemented in the source code of the circuit simulator SPICE2 to create SOISPICE-2, a semi-numerical device/circuit simulator, which can be effectively used as a design tool for thin-film SOI CMOS ICs. The detailed model algorithm and numerical techniques chosen to increase the computational efficiency and to alleviate convergence problems of SOISPICE-2 are described. DC simulations for half-micron thin-film SOI MOSFETs are compared with corresponding measurements and numerical device simulations done with PISCES to provide some support for the model. The utility and the efficiency of SOISPICE-2 are demonstrated through representative device and circuit simulations.

CHAPTER 1
INTRODUCTION

Silicon-on-insulator (SOI) MOSFET technology has been known to provide various potential advantages in applications to very large scale integration (VLSI) [Wea87, Lam87]. It provides increased radiation hardness due to a smaller volume for carrier generation, and a speed advantage due to the low parasitic capacitance associated with smaller junction areas resulting from the presence of the underlying insulating layer with lower permittivity than silicon. The afforded capability of simple but complete electrical isolation of silicon regions portends the elimination of latch-up, which plagues bulk CMOS, and an increase in packing density. This capability also makes SOI suitable for high-voltage applications since high-voltage and low-voltage devices can be integrated but isolated on the same chip. The structure of SOI also provides a flexibility for 3-D device integration. These potential advantages indeed seem to render SOI technology truly competitive with contemporary bulk silicon technology.

Full depletion of the silicon film has been known to provide additional benefits for VLSI. These include

elimination of short-channel effects [Vee89], elimination of floating-body effects [Col88], reduction of high-field problems [Col87a], enhanced current drive capability and transconductance [Stu88], and better subthreshold characteristics [Col86, Wou90]. Considering these benefits afforded by thin-film devices, the SOI technology must be a strong contender for future deep-submicron CMOS applications. Nevertheless no one has yet been successful in fabricating fully depleted submicron SOI CMOS circuits which show expected performances. It is a fact that this technology has not yet been practically proven to be a serious contender for submicron CMOS.

For SOI to become truly competitive with the established bulk silicon CMOS technology, unique benefits must be exploited. SOI MOSFETs are unique because they are fabricated in thin silicon films, with charge-coupled front and back (substrate) gates [Lim83, Lim84] (see Fig. 1.1). As the device dimension is shrinking to increase the packing density and device speed, drain-field-related problems are getting more serious. The high drain field produces electrons with high energy, i.e., hot electrons. These hot electrons can surmount the potential barrier at the silicon-oxide interface and create oxide charge and interface states that degrade device performance [Hu85]. While this long-term reliability is one of the main concerns in submicron bulk MOSFET design,

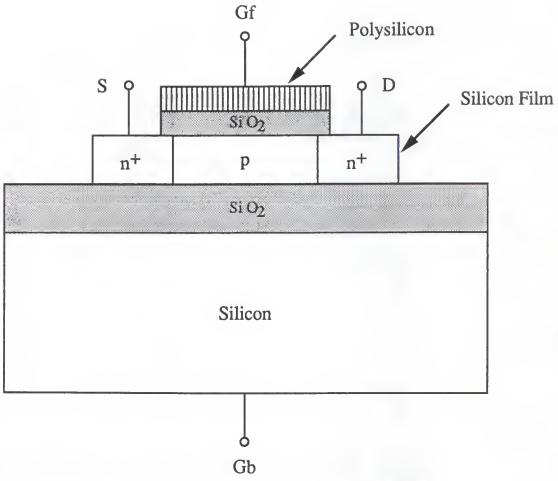


Fig. 1.1 Cross-sectional view of a floating-body n-channel SOI MOSFET structure showing the four terminals: the front gate (Gf), the back gate (Gb), the source (S), and the drain (D).

SOI seems to have more flexibility in design due to the presence of the underlying oxide layer.

However, unlike the bulk MOSFET, the SOI MOSFET body floats (actually or virtually because of high body resistance), and hence the concomitant floating-body effects must be recognized and suppressed if detrimental. Fully depleted SOI MOSFETs have been considered to be free of the kink effect [Col88], but the underlying physics, which also relates to the BJT action, has not been adequately analyzed. Such analysis is needed to understand the BJT-induced breakdown [You88] and latch phenomena [Che88], which portend power-consumption problems in SOI CMOS. Although the published studies of these effects involve only bulk-like (partially depleted) SOI devices, they can occur in fully depleted devices [Mck89]. The SOI technology seems to provide more flexibility in design, but higher complexity at the same time.

While there has been a continuous improvement in SOI film quality and process technique, there has been little work [Aok89] done for design optimization, and no standard design rule for fully depleted SOI MOSFET has been defined. This is due to lack of understanding of unique features in these devices, such as parasitic BJT effects, back-channel leakage by drain-induced barrier lowering (DIBL), and dependence of drain field on device structure. To realize the potential benefits afforded by SOI technology in submicron

CMOS VLSI, study on design optimization of fully depleted SOI MOSFET is essential.

Some modeling efforts have been done to analyze the unique features of the fully depleted SOI MOSFET. Among these, the accumulated works done by Lim [Lim83, Lim84, Lim85] and Veeraraghavan [Vee88b, Vee89] have been fruitful and have resulted in successful implemention of a quasi-static large-signal model for the short-channel fully depleted SOI MOSFET into the circuit simulator SPICE2 [Nag75]. Even though this simulator, SOISPICE [Fit89], is the most useful SOI simulator available, it does not consider recently acknowledged important characteristics of SOI devices with submicron channel length, such as parasitic BJT effects and back-surface DIBL leakage. These phenomena must be accounted for to render the simulator truly useful for CAD based on contemporary SOI CMOS technology involving fully depleted floating-body devices.

Contemporary short-channel MOSFET technology uses the lightly doped-drain (LDD) structure to reduce overall short-channel effects associated with the high drain field. An identical lightly doped-source (LDS) structure is usually included to simplify the technology. Our study on device optimization concludes that both the LDS and LDD are essential for fully depleted submicron SOI MOSFET technology, as we will discuss in this dissertation. Even though there has been some work done to model the effects of the LDD in

bulk MOSFETs [May87, Ter84], little effort has been made to include the effects of LDD and LDS in models for circuit simulation. An advanced device/circuit simulator should have a capability to simulate effects of LDD and LDS, which are also missing in SOISPICE.

This dissertation, then, is concerned with design optimization of the fully depleted submicron SOI MOSFET, and development of a physical model including the unique features of the fully depleted SOI MOSFET. This work will provide a design strategy through physical explanations of unrecognized unique features in the fully depleted submicron SOI MOSFET, and an advanced device/circuit simulator, SOISPICE-2, which will be useful for the design of fully depleted SOI CMOS VLSI. The main contributions made in the work are as follows:

(1) formulation of a strategy for optimal design of fully depleted submicron SOI CMOS based on analyses of high drain field problems and floating-body effects;

(2) application of the LDS concept to device design by analyzing unrecognized LDS effects on device characteristics;

(3) development of a comprehensive physical model for the fully depleted SOI MOSFET;

(4) implementation of the developed model in the source code of SPICE2, creating the new device/circuit simulator SOISPICE-2.

In Chapter 2, using a previously developed physical model [Vee88b] (written into the SPICE2 source code [Fit89])

for the SOI MOSFET, we examine device design to exploit the unique benefits in CMOS VLSI. The figure of merit emphasized is hot-carrier-induced degradation, monitored by the impact-ionization current generated near the drain. Simulations, supported by measurements of devices fabricated in SIMOX films, suggest that the (short-channel) SOI MOSFET can be designed to suppress the degradation much below that in a contemporary bulk MOSFET which includes an LDD. This unique benefit, which results for moderate (not ultra-thin) film thickness with complete depletion in the film and at the back surface, is due to the control of the electric field by the front gate-back gate charge coupling. The optimal design involves tradeoffs, which are discussed.

Prevalent floating-body effects, which are triggered by impact-ionization charging of the film body, are the "kink" effect [Kat85], and effects associated with the parasitic bipolar junction transistor (BJT), which can be detrimental in CMOS applications and must be constrained. These floating-body effects are difficult to analyze by device measurements since biasing the body, for example, to monitor the impact-ionization current, will disturb the potential distribution inside the device. In Chapter 3, we analyze the floating-body bipolar effects in the fully depleted submicron SOI MOSFET, relying on copious two-dimensional device simulations for insight. We focus on the BJT effects, but begin with a physical explanation of the disappearance of the kink in the

fully depleted device. Parametric dependences are examined to give physical insight for optimal design. The analysis further relates the DC breakdown and latch mechanisms in the fully depleted submicron SOI MOSFET to the actual BJT-induced problems in an operating SOI CMOS circuit. A comprehensive understanding of the floating-body effects is attained, and a device design to control them is suggested and shown to be viable. The design is based on the use of an LDS to suppress the current gain of the BJT.

In Chapter 4, we develop a comprehensive semi-numerical model for the fully depleted SOI MOSFET, which is aimed at providing an advanced device/circuit simulator for the design of fully depleted SOI CMOS VLSI. In this development, most of the important phenomena and provisions, which are missing in the previous model [Vee88b], are included. We derive models for the subthreshold current at both front and back surfaces, the parasitic BJT current, the recombination current at the source-body junction, the effects of LDS and LDD regions, and the thermal generation leakage current in the fully depleted SOI MOSFET. These models are derived with the physical insights gained from the analyses based on PISCES simulations. The derivation exploits a proper linkage to the previously developed short-channel SOI MOSFET model [Vee88b].

In Chapter 5, the model implementation in the new simulator SOISPICE-2 is described in detail. Detailed software development, based on the optimized model algorithm,

is discussed. The numerical techniques chosen to increase the efficiency of the simulator are described. Simplifications of the model and their limitations are also discussed. The capability and efficiency of the simulator as a semi-numerical mixed-mode device/circuit simulator for technology CAD is demonstrated in this chapter.

In Chapter 6, the main accomplishments of this dissertation are summarized, and suggestions of areas for future work are made.

In Appendix, the equivalent version of the main model routine in SOISPICE-2, which is a complete FORTRAN program for DC simulations of fully depleted floating-body SOI MOSFETs, is listed to facilitate future modifications or enhancements of the model.

CHAPTER 2
DESIGN FOR LONG-TERM DEVICE RELIABILITY

2.1 Introduction

Thin-film silicon-on-insulator (SOI) technology is potentially advantageous for CMOS VLSI because of the simple isolation afforded. However for SOI to become truly competitive with the established bulk silicon CMOS technology, unique benefits must be exploited. The SOI MOSFET is unique because it is fabricated in a thin silicon film, with charge-coupled front and back (substrate) gates [Lim83, Lim84]. Previous work has demonstrated that the thin-film SOI MOSFET does indeed have advantages over the bulk MOSFET, including ameliorated short-channel effects [Col87b, Vee89], enhanced current drive and transconductance [Stu88, Yosh87], and reduced hot-carrier effects [Col87a].

Using a previously developed physical model [Vee88b] (written into the SPICE2 source code [Fit89]) for the SOI MOSFET, we examine in this chapter device design to exploit the unique benefits in CMOS VLSI. The figure of merit emphasized is hot-carrier-induced degradation, monitored by the impact-ionization current generated near the drain. Simulations, supported by measurements of devices fabricated

in SIMOX films, suggest that the (short-channel) SOI MOSFET can be designed to suppress the degradation much below that in a contemporary bulk MOSFET which includes an LDD. This unique benefit, which results for moderate (not ultra-thin) film thickness with complete depletion in the film and at the back surface, is due to the control of the electric field by the front gate-back gate charge coupling. It can extend the use of the 5-V power supply in submicron SOI CMOS, whereas the bulk technology is being forced to 3.3 V. The optimal design involves tradeoffs, which are discussed.

2.2 Analysis

Through simulations supported by measurements of test devices, optimal designs of SOI MOSFETs to exploit their uniqueness for CMOS VLSI applications are discussed in this section. The designs, for maximum hot-carrier-induced degradation lifetime of the n-channel device, are evolved systematically, using physical insight for interpretation of the data generated.

2.2.1 Simulations

The simulations to be described were done with an enhanced version of SPICE2 [Fit89], in which the previously developed physical SOI MOSFET model [Vee88b] has been implemented. The five-terminal model applies to the fully depleted device and allows for charge sheets at the front

(channel) and back silicon surfaces. The back surface is assumed to be either accumulated (TFA) or depleted (TFD) everywhere between the source and the drain. The model physically accounts for the predominant short-channel effects in MOSFETs (i.e., threshold-voltage reduction, drain-induced conductivity enhancement (DICE), velocity saturation with mobility degradation, and channel-length modulation) as influenced by the unique features of thin SOI devices (i.e., the presence of the coupled back gate and the possibility of a floating film body) [Vee89]. It includes characterization of generation current due to (weak) impact ionization in the high-field channel region near the drain, with the multiplication factor controlled by all terminal voltages.

We first consider which mode of operation, TFA or TFD, is better. Note that other modes of operation are possible, but are not desirable. The back surface should not be inverted to avoid undue leakage current, nor should it be partially accumulated and depleted to avoid undue device-to-device variations. In the TFA mode, the transverse electric field in the film tends to be high to support the channel charge and the back-surface accumulation charge. Consequently, the threshold voltage tends to be high and the channel current and transconductance tend to be low [Lim83, Lim84]. From the TFA model [Vee88b], $V_{Tf} \propto 1/t_b$ and $I_{DS(sat)} \propto t_b$ when t_b, the film thickness, is sufficiently thin. Thus the reduced current drive is exacerbated as t_b is scaled down,

which is necessary to realize the amelioration of short-channel effects in the SOI MOSFET [Vee89].

The TFA mode of operation furthermore enables the kink effect [Col88], and related floating-body effects which are undesirable. These effects result when majority carriers, generated for example by impact ionization, are injected into the film body and stored in the accumulation layer at the back surface. This charge modulation forward-biases the source junction and thereby enhances the channel charge and current at a given gate bias.

Finally, the longitudinal electric field in the channel at the drain, related to the high transverse field, is abnormally high in the TFA mode, and consequently the hot-carrier effects are severe. To first order, the longitudinal field at the drain varies inversely with t_b [Vee88b], and hence the effects are worse in scaled devices. Additionally, the high field (in both directions) results in mobility degradation and premature current saturation due to velocity saturation [Vee88b].

The undesirable features associated with the TFA mode of operation will be demonstrated by simulations and measurements later in this section. Because of them however, our study of the optimal SOI MOSFET design will now focus on the TFD mode of operation. This mode has been shown previously [Col87a, Col87b, Stu88, Vee89, Yosh87], to offer advantages with regard to short-channel effects, current-

drive, and hot-carrier-induced degradation. Furthermore, the TFD mode tends to suppress the floating-body effects [Col88] because of the depletion condition that is maintained under the channel. The previous work has not given adequate explanation of the benefits afforded by TFD operation, nor have the tradeoffs for design optimization been defined. In doing so herein, we will find that it is possible in the TFD mode to control the electric field near the drain, and hence to govern the hot-carrier effects.

We first discuss results of nominal TFD and TFA device simulations, and compare them with representative bulk device characteristics. To maintain a standard of reference, the bulk device was simulated via a TFA model with t_b set equal to the depletion-region width, $x_{d(max)}$, at strong inversion. This is a good representation since the depletion (body) capacitance C_d of this particular TFA device equals that of the bulk device at the source. In essence we are approximating the bulk-device characteristics based on the assumption that $C_d = \varepsilon_s/x_{d(max)}$ is constant along the channel. This assumption is commonly used in bulk MOSFET models. For all simulations, the body was tied to the source to monitor the impact-ionization (viz., body) current. In the floating-body mode of operation, which is desirable for real applications, the TFD device characteristics are virtually identical to those predicted by these simulations provided the parasitic bipolar transistor is insignificant. For the

TFA device, the shorted-body simulations miss the reduction of hot-carrier effects due to the floating-body charging (which also produces the kink effect) [Col87a]. This neglect does not compromise our analysis however since the floating-body effects as a whole are undesirable and would probably be avoided in an optimal design.

The simulated current-voltage characteristics for n-channel devices having 1.0-μm channel lengths are shown in Fig. 2.1. Since the threshold voltage varies from one device to the next, each set of curves corresponds to a fixed value for $(V_{GfS}-V_{Tf})$. The body doping density N_A was 5×10^{16} cm^{-3}, the (front) gate-oxide thickness t_{of} was 20 nm, and the back gate-oxide thickness t_{ob} was 450 nm. For the thin-film devices (TFD and TFA), t_b was 100 nm; for the bulk device, t_b = $x_{d(max)}$ = 140 nm. The superiority of the TFD device with regard to $I_{DS(sat)}$ is apparent in Fig. 2.1.

As mentioned previously, this superiority is due to charge coupling in the thin-film devices. From the model [Vee88b], we can approximate [Vee89]

$$I_{DS(sat)} \cong \frac{W\,\mu_{eff}\,C_{of}}{2L_e(1+\alpha)}\,[V_{GfS} - V_{Tf(eff)}]^2 \qquad (2.1)$$

where $\alpha = C_b/C_{of}$ or $C_bC_{ob}/(C_b+C_{ob})C_{of}$ for the TFA and TFD modes respectively; $C_b = \varepsilon_s/t_b$ is the body capacitance, and C_{of} and C_{ob} are the front and back gate-oxide capacitances. In (2.1), $V_{Tf(eff)}$ is a mathematically defined effective threshold

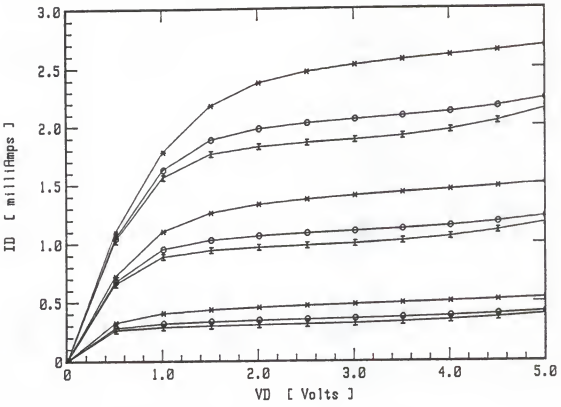


Fig. 2.1 Simulated I_{DS}-V_{DS} characteristics of TFD (*), TFA (I), and bulk (O) devices, with (V_{GfS}-V_{Tf}) = 1, 2, and 3 V. All simulated devices are n-channel with L = 1.0 μm and W = 10.0 μm.

voltage, which is lower than the actual V_{Tf} for short-channel devices because of drain-induced conductivity enhancement (DICE) [Vee88b, Vee89]. Note that for TFA, $\alpha \propto 1/t_b$, whereas for (typical) TFD, α is much less than unity. (Also note that for bulk devices, α in the $I_{DS(sat)}$ expression analogous to (2.1), derived via the constant-C_d assumption, is replaced by the ratio of C_d to the oxide capacitance; this is the basis for our TFA representation of the bulk MOSFET.) Thus (2.1) explains the different characteristics in Fig. 2.1.

Included in the simulated drain currents in Fig. 2.1 is the weak impact-ionization current,

$$I_{Gi} = (M-1)\, I_{DS(sat)} \quad , \tag{2.2}$$

generated in the high-field region near the drain. The multiplication factor in the model, derived [Vee88b] by integrating the ionization coefficient over this region, depends on both the drain and gate voltages:

$$M-1 = \frac{\alpha_0}{\beta_0} [V_{DS}-V_{DS(eff)}] \exp\left[-\frac{\beta_0 l_c}{V_{DS}-V_{DS(eff)}}\right] \tag{2.3}$$

where

$$l_c = t_b \left[\frac{C_b \beta}{2C_{of}(1+\alpha)}\right]^{1/2} \tag{2.4}$$

is a characteristic length that depends on t_b and the back-surface charge condition via α and β; $\beta = 1$ or $1 + C_b/(C_b+C_{ob})$ for TFA and TFD respectively. In (2.3), $V_{DS(eff)}$, which is approximately $V_{DS(sat)}$, depends on the back-surface charge condition as well: $V_{DS(eff)} \propto 1/(1+\alpha)$. (Note that the decrease of $V_{DS(sat)}$ due to carrier velocity saturation in short-channel MOSFETs is a prime reason for enhanced impact ionization and degradation in scaled devices.) In (2.3), α_0 and β_0 are impact-ionization constants for electrons assumed to be 1.4×10^6 cm^{-1} and 2.6×10^6 V/cm respectively [Elm77]. The modeling of I_{Gi} is important because it can be correlated with the MOSFET lifetime τ defined by hot-carrier-induced degradation of the gate oxide. For the static case [Hu85],

$$\tau \propto \frac{W}{I_{DS}} (M-1)^{-m} \qquad (2.5)$$

where $m \cong 3$. Note that the (M-1) factor in (2.5) is a proper monitor in relative comparisons of τ for different devices operating at the same current per unit width.

In Fig. 2.2, we plot simulated (M-1) versus V_{DS} for the devices of Fig. 2.1. For each bias point, (M-1) was evaluated from (2.2) with I_{Gi} being the predicted body current. For all the plots, $(V_{GfS}-V_{Tf}) = 1.5$ V, where I_{Gi} is maximum for fixed V_{DS}. The reduced multiplication and thus the longer τ implied by (2.5) afforded by the TFD device are dramatic. This benefit of TFD, and the obvious inferiority of TFA with

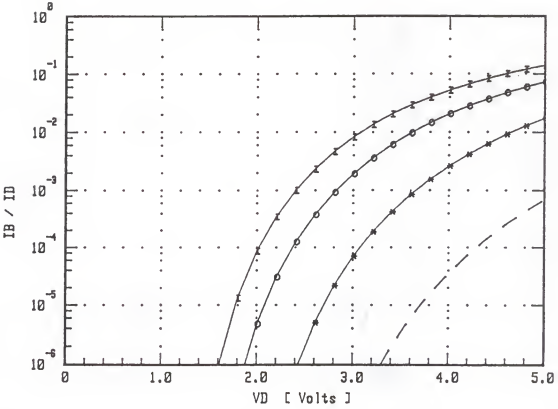


Fig. 2.2 Simulated (M-1) versus V_{DS} for devices in Fig. 2.1: TFD (*), TFA (I), and bulk (O). The simulated characteristic for the thicker (t_b = 300 nm) TFD device (dashed curve) is included. For all simulations, (V_{GfS}-V_{Tf}) = 1.5 V.

regard to τ result because of the control of the electric field provided by the front surface-back surface charge coupling in the thin-film SOI MOSFET. This control is reflected in (2.3) by l_c and $V_{DS(eff)}$, which depends on α and β and hence on the back-surface charge condition. The strong (inverse) dependence of (M-1) on t_b results from the fact that less lateral displacement (electric field) is needed to support a given (channel) charge in a thicker (two-dimensional-field) region.

With the insight provided by (2.3)-(2.5) and the results in Fig. 2.2, we now consider optimizing the TFD design through simulations to minimize (M-1). Such optimization would suggest use of the SOI TFD device structure, without an LDD, for short-channel CMOS VLSI having acceptable lifetime while retaining the 5-V supply voltage. We increase t_b to 300 nm and reduce N_A to $5x10^{15}$ cm^{-3} to maintain the fully depleted condition in the film. The threshold voltage is reduced, but could be maintained by using a thicker gate oxide defined by tradeoffs involving transconductance (see (2.1)), short-channel effects, and oxide immunity [Yos85]. Note that all of these parametric changes tend to decrease (M-1) as modeled in (2.3), and hence increase τ in (2.5). The most effective change is the t_b increase, which is why this sort of "design for τ" flexibility is afforded by SOI and not by the bulk technology. For better control of V_{Tf}, a different gate material could be used, e.g., p^+ polysilicon or metal

silicide. The simulated (M-1) for this thicker TFD device is compared with the previous simulation in Fig. 2.2. A significant reduction is predicted. Note that for the assumed $(V_{GfS}-V_{Tf})$, (M-1) of the thicker TFD device at V_{DS} = 5 V equals that of the bulk device (TFA with $C_b = \varepsilon_s/x_{d(max)}$ and without an LDD) at V_{DS} = 2.7 V. Although not shown, the simulated (M-1) for the thicker device in the TFA mode is also significantly lower than that for the thinner TFA device in Fig. 2.2.

To see the effects of varying t_{ob} in a short-channel (1-μm) TFD MOSFET, we show in Figs. 2.3 and 2.4 simulations of I_{DS} and (M-1), respectively, for a variety of devices with N_A = $5x10^{15}$ cm^{-3}. The current-voltage characteristice are relatively insensitive to variations in t_b and t_{ob}. This is advantageous because of possible unavoidable fluctuations in these thicknesses in an actual SOI wafer. The weak dependence of $I_{DS(sat)}$ on t_b seen in Fig. 2.3 is due to channel-length modulation and DICE [Vee88b]. These short-channel effects, which increase the channel conductance as V_{DS} increases, become more significant as t_b increases [Vee89]. In Fig. 2.4, (M-1) is not strongly dependent on t_{ob}, but is affected dramatically by changes in t_b as explained above. The predicted dependences are consistent with the insight provided by (2.1)-(2.5); (M-1) is reduced and τ is lengthened as t_b is increased. Because of the short-channel effects, design tradeoffs are implied. The optimal t_b is an upper

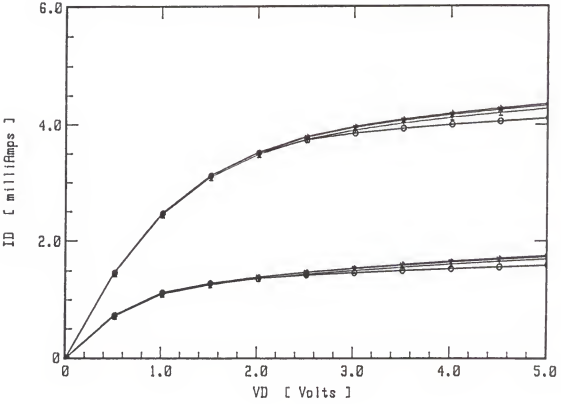


Fig. 2.3 Simulated TFD I_{DS}-V_{DS} characteristics, with V_{GfS} = 2 and 4 V, for various t_{ob} and t_b: t_b = 300 nm and t_{ob} = 450 nm (*); t_b = 300 nm and t_{ob} = 300 nm (I); t_b = 300 nm and t_{ob} = 600 nm (+); t_b = 150 nm and t_{ob} = 450 nm (O).

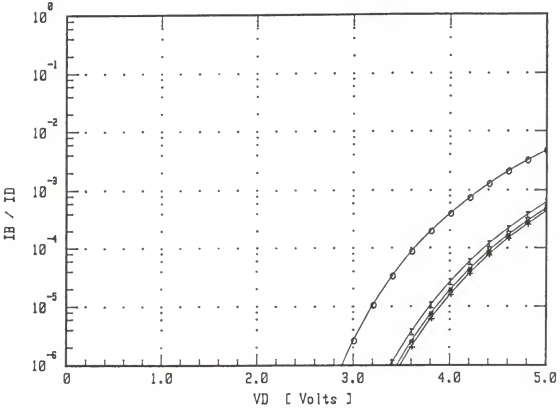


Fig. 2.4 Simulated TFD (M-1) versus V_{DS} for devices in Fig. 2.3 (same symbols) with V_{Gfs} = 2V.

limit defined by acceptable short-channel effects, or by the fully depleted-film requirement, which depends on the minimmum N_A achievable and V_{Tf} needed.

All the simulations discussed above are for devices without an LDD region. In the contemporary bulk technology, an LDD is commonly used to reduce the electric field near the drain and thereby suppress the hot-carrier effects. (To first order, replacing l_c by (l_c+L_{LDD}) in the analysis underlying (2.3) and (2.4) characterizes the field reduction [HU85].) Typically (M-1) is reduced about an order of magnitude by the LDD in the bulk device [Ter84]. From the data in Fig. 2.2, we can see that an optimal TFD MOSFET, without an LDD, can indeed suppress (M-1), and hence lengthen τ substantively relative to the bulk device having an LDD. We infer from the simulations that the thicker TFD MOSFET at V_{DS} = 5 V yields (M-1) comparable to that for the typical bulk MOSFET, with an LDD, at V_{DS} = 3.3 V. These results imply a significant unique benefit afforded by SOI CMOS VLSI which could render the technology truly competitive with bulk CMOS.

2.2.2 Measurements

Measurements were made on TFD, TFA, and bulk-like SOI test devices. All the devices included an LDD, unlike the simulations, but the results clearly support the design implications of our analysis.

The n-channel MOSFETs were built on SIMOX substrate with a 280-nm silicon film and an underlying 400-nm silicon-dioxide layer. The devices were fabricated using a conventional CMOS process, with a reach-through implant to form the LDD regions. Three device structures, A, B, and C, were used. For device A, W = 1.8 μm, L = 1.25 μm, t_{of} = 25 nm, and $N_A = 1x10^{16}$ cm^{-3}. Device B is identical to device A except that $N_A = 8x10^{16}$ cm^{-3} is higher. For device C, W = 3.6 μm, L = 1.2 μm, t_{of} = 20 nm, and $N_A = 1x10^{17}$ cm^{-3}.

Because of the higher doping density, devices B and C are bulk-like. Device A can be operated in either the TFD or the TFA mode, depending on the back-gate bias V_{GbS}. To ensure TFA, V_{GbS} = -10 V; to ensure TFD, V_{GbS} = +10 V, well below the back-gate threshold voltage. The body terminal of each device was grounded to the source to monitor I_{Gi}. The (front-gate) threshold voltages of TFD, TFA, and the bulk-like devices B and C are 0.25 V, 0.28 V, 1.03 V, and 1.04 V respectively.

The measured I_{DS}-V_{DS} characteristics of TFD, TFA, and device B are shown in Fig. 2.5. Fixed (V_{GfS}-V_{Tf}) values are used again as for the simulations. The predicted improvement of $I_{DS(sat)}$ is obvious with the mode change from TFA to TFD. $I_{DS(sat)}$ of bulk device B is much lower than that of the TFA device mainly because of the lower electron mobility due to the higher doping density. This implies another advantage of lightly doped TFD devices.

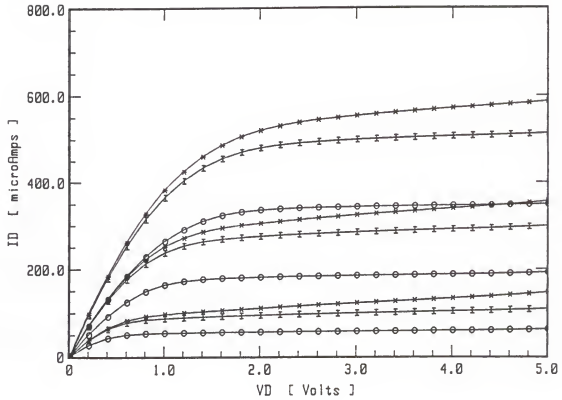


Fig. 2.5 Measured I_{DS}-V_{DS} characteristics of fully depleted and bulk-like SOI devices with (V_{GfS}-V_{Tf}) = 1, 2, and 3 V: device A in TFD mode (*); device A in TFA mode (I); and bulk device B (O).

In Fig. 2.6, we plot measured (M-1) versus V_{DS} for the devices in Fig. 2.5, as well as for bulk-like device C with thinner gate oxide. For all the plots, $(V_{GfS}-V_{Tf})$ = 1.5 V, which is where I_{Gi} is maximum for V_{DS} = 5 V. The predicted reduction of (M-1) is obvious with the mode change from TFA to TFD. The superiority of the TFD device over the bulk devices is also evident. Note the higher (M-1) due to the thinner t_{of} of device C. The measured improvement afforded by the TFD device over the TFA and bulk devices is smaller than that predicted by the previous simulation in Section 2.2.1. This discrepancy could be due to the presence of the LDD in the test devices. The LDD is probably more effective in reducing the drain field in device B than device A since the same implant dose and energy ($2x10^{13}$ cm^{-2}, 100 KeV) were used, and hence a lower (more effective) net LDD doping density in device B. The theoretical-experimental discrepancy could also be explained by (a) the absence of back-surface accumulation near the drain in TFA test device and/or (b) the channel-current spreading in the high-field region near the drain in the test devices, which is unaccounted for in the simulations based on (2.2). Even though exact comparison cannot be made because of the presence of the LDD in the test devices, the measured data in Figs. 2.5 and 2.6 support the analysis and the implied significant benefits afforded by an optimally designed TFD MOSFET.

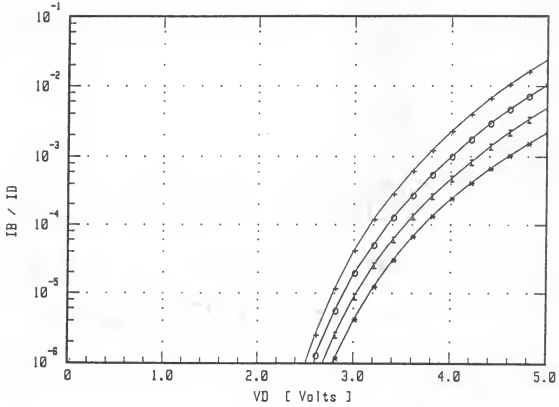


Fig. 2.6 Measured (M-1) versus V_{DS} for devices in Fig. 2.5: TFD (*), TFA (I), and bulk device B (O). The characteristic for bulk device C (+) with thinner t_{of} is included. For all measurements, $(V_{Gfs}-V_{Tf})$ = 1.5 V.

2.3 Discussion

The simulations and measurements described clearly show a unique advantage of SOI over bulk CMOS VLSI with regard to hot-carrier-induced degradation (of the n-channel MOSFET). A properly designed short-channel TFD MOSFET, with moderately thin (not ultra-thin) film and light channel doping to ensure complete depletion of the film and back surface, could, without an LDD, have a lifetime at 5 V comparable to that of a bulk MOSFET with an LDD at 3.3 V.

However design tradeoffs, involving other device characteristics, must be considered to ensure the viability of the suggested SOI/TFD CMOS technology. The other characteristics that obviously will be involved relate to threshold voltage, short-channel effects including punchthrough, and the parasitic bipolar transistor. The TFD design tends to reduce the threshold voltage, but the tradeoff implied can be loosened by using a p^+-polysilicon or metal-silicide gate rather than the conventional n^+ gate. Also with regard to threshold voltage, a thicker gate oxide could be used, given the increased transconductance afforded by the TFD mode of operation, which further reduces the hot-carrier effect.

Short-channel effects in the proposed TFD SOI design would seem to be significant because of the lower channel doping density. However thin-film SOI tends to ameliorate short-channel effects [Vee89], even for low channel doping as

reflected by the simulations and measurements reported herein. Nevertheless punchthrough, which is a critical problem in submicron bulk MOS technology, would seem to be problematical in submicron TFD SOI as well because of the complete depletion and the lower channel doping requirements. However, we have not seen significant punchthrough in submicron (~1 μm) TFD devices we have measured, in accord with results in [Yosh87]. Indeed punchthrough, which is related to DICE [Vee88b], or drain-induced barrier lowering, can be controlled in thin-film SOI by exploiting the front gate-back gate coupling to control the two-dimensional electric field in the film, as can other short-channel effects [Vee89].

The parasitic bipolar transistor, which can be activated by charge injection into the body, for example via impact ionization, is potentially a problem in submicron MOS because the current gain tends to be high. In contrast to the bulk technology, the SOI body should float (although it could be tied to the source in a more complex technology), and hence the BJT can potentially operate in an open-base mode. In the next chapter, we analyze this potential problem with the floating body to suggest a device design to control it in submicron thin-film SOI CMOS VLSI.

CHAPTER 3
ANALYSIS AND CONTROL OF FLOATING-BODY BIPOLAR EFFECTS

3.1 Introduction

In Chapter 2, we demonstrated the potential superiority of the SOI MOSFET with regard to hot-carrier-induced degradation, which can be constrained in the fully depleted, moderately (not ultra-) thin device because of the dependence of the drain electric field on the film thickness. However, unlike the bulk MOSFET, the SOI MOSFET body floats (actually or virtually because of high body resistance), and hence the concomitant floating-body effects must be recognized and suppressed if detrimental.

The prevalent floating-body effects, which are triggered by impact-ionization charging of the film body, are the kink effect [Kat85], which is not harmful but is undesirable because of the abnormality it creates, and effects associated with the parasitic bipolar junction transistor (BJT), which can be detrimental in CMOS applications and must be constrained. Fully depleted SOI MOSFETs have been considered to be free of the kink effect [Col88], but the underlying physics, which also relates to the BJT action, has not been adequately analyzed. Such analysis is needed to understand

the BJT-induced breakdown [You88] and latch phenomena [Che88], which portend power-consumption problems in SOI CMOS. Although the published studies of these effects involve only bulk-like (partially depleted) SOI devices, they can occur in fully depleted devices [Mck89]. In this chapter, we analyze the floating-body bipolar effects in fully depleted submicron SOI MOSFETs, relying on copious two-dimensional device simulations for insight. We focus on the BJT effects, but begin with a physical explanation of the disappearance of the kink in the fully depleted device. Parametric dependences are examined to give physical insight for optimal design. The analysis further relates the DC breakdown and latch mechanisms in the fully depleted submicron SOI MOSFET to the actual BJT-induced problems in an operating SOI CMOS circuit. A comprehensive understanding of the floating-body effects is attained, and a device design to control them is suggested and shown to be viable. The design is based on the use of a lightly doped source (LDS) incorporated with a self-aligned silicide-contact technology to suppress the current gain of the BJT.

3.2 Analysis

We analyze first the kink effect, and then the (npn) parasitic BJT effects in the fully depleted floating-body submicron n-channel SOI MOSFET. Two-dimensional device simulations done with PISCES [Tma89] aid the analyses. This

simulator includes physical models for doping- and field-dependent carrier mobility with velocity saturation and surface mobility degradation (20 %), Shockley-Read-Hall (SRH) recombination/generation with doping-dependent lifetime

$$\tau = \frac{\tau_0}{1 + N/5\text{x}10^{16}\text{cm}^{-3}} \quad , \tag{3.1}$$

Auger recombination, bandgap narrowing, and impact ionization with electric field (E)-dependent coefficients $\alpha = \alpha_0 \exp(-\beta_0/E)$. The SOI device structure simulated, illustrated in Fig. 3.1, had virtual step (n^+p) source and drain junctions reaching the underlying Si-SiO_2 interface. (The simulated drain electric field could thus be more intense than that in an actual device with a less abrupt drain-body junction, e.g., one with an LDD.) Unless otherwise mentioned, all simulations used a (front) gate-oxide thickness of 20 nm, a buried oxide thickness of 400 nm, source and drain doping levels of $5\text{x}10^{19}$ cm^{-3}, a substrate thickness of 2 μm; the gate material was specified as n^+ polysilicon.

3.2.1 Kink Effect

The kink seen in the saturation-region I_{DS}-V_{DS} characteristics of floating-body SOI MOSFETs is a result of the decrease in the (front-channel) threshold voltage V_{Tf} caused by forward-biasing of the source-body junction. Impact ionization in the high-drain-field region injects holes into

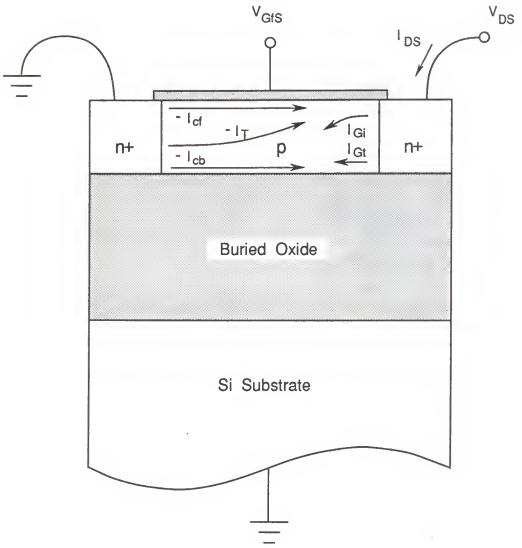


Fig. 3.1 SOI n-channel MOSFET structure, including indications of various current components.

the floating body, and the concomitant stored charge induces the forward bias. This effect has been shown to be negligible in fully depleted devices [Col88]. The primary explanation given [Col88] for this suppression of the kink is that since the source-body potential barrier is small in the depleted film, excess hole accumulation (and hence the forward-biasing) is prevented. It might thus be inferred from this explanation that the BJT effects are also suppressed in the fully depleted SOI MOSFET since the forward bias drives the BJT base-emitter junction. This is not the case as we shall see, and hence a more detailed explanation is needed.

We simulated three floating-body devices, A, B, and C, having different film thicknesses, t_b = 140 nm, 100 nm, and 50 nm, respectively. The channel length L is 0.5 μm, the (uniform) body doping N_A is 6×10^{16} cm^{-3}, which defines the theoretical maximum depletion-region width, $x_{d(max)}$ = 130 nm. The SRH lifetime parameter τ_0 in (3.1) is 100 nsec. The substrate and the source were grounded for the simulations as illustrated in Fig. 3.1. Figure 3.2 shows the I_{DS}-V_{DS} characteristics of these devices at fixed $(V_{GfS}-V_{Tf})$ = 2 V. Notice only device A, the thickest device, shows a discernible kink. These results are then consistent with the theory that full depletion suppresses the kink; device A in fact is not truly fully depleted ($t_b > x_{d(max)}$). However closer examination of the simulation results reveals a flaw in the explanation cited [Col88], as we now discuss.

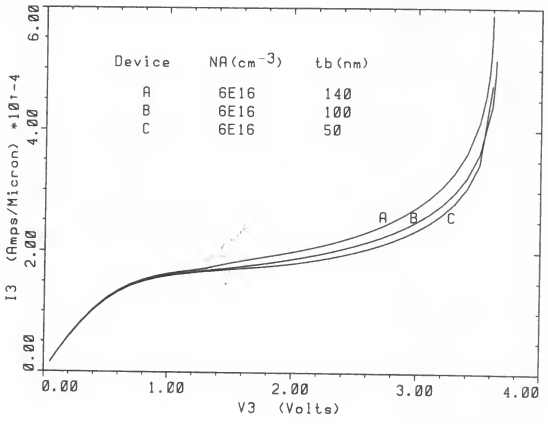


Fig. 3.2 PISCES-simulated I_{DS}-V_{DS} characteristics with (V_{GfS}-V_{Tf}) = 2 V. For all devices, L = 0.5 μm and τ_0 = 100 ns. In the figure, V3 and I3 denote V_{DS} and I_{DS} respectively.

From the output files of the simulations, we extracted the source-body potential barriers, ϕ_{bs}, at the back interface. These barriers are plotted versus V_{DS} in Fig. 3.3. Note that the thickest device A shows the largest barriers, which is diminished abruptly at $V_{DS} \approx 1.3$ V. This is where the kink in Fig. 3.2 occurs. The barriers in devices B and C are smaller, and do not change significantly as V_{DS} increases. These results seem consistent with the explanation referred to above. However, the explanation is inconsistent with Fig. 3.4, where we plot versus V_{DS} the predicted separation of quasi-Fermi potentials in the source-body junction at the back interface. The separation,

$$V_{BS} = \phi_p - \phi_n \tag{3.2}$$

can be considered the forward bias on the source-body junction; it defines the pn-product at the junction and thus reflects the carrier injection level. Note in Fig. 3.4 that even in the thinner devices that do not show a kink, V_{BS} increases to >0.9 V as V_{DS} increases, and in fact is higher than that in the thicker device. This can be explained by the fact that the higher drain field in the thinner devices causes more impact-ionization current, which must be equalized by higher recombination rates that vary as $\exp(V_{BS}/nV_{th})$, where V_{th} is the thermal voltage. Furthermore

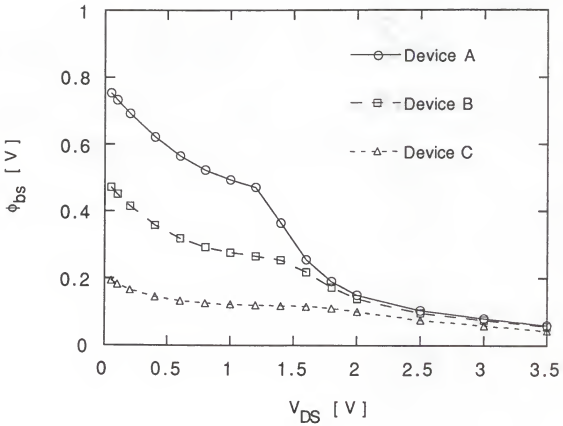


Fig. 3.3 Predicted source-body potential barriers at the back interface for devices in Fig. 3.2.

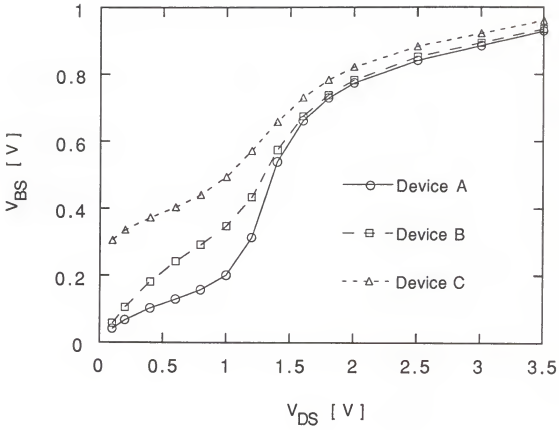


Fig. 3.4 Predicted quasi-Fermi-level separation in the source-body junction at the back interface for devices in Fig. 3.2.

the recombination is constrained to thinner regions (smaller volumes), which means even higher V_{BS} is needed.

In addition, another mechanism heretofore unrecognized was found to cause V_{BS} to be higher in thinner devices, especially at lower V_{BS} values. The impact-ionization current I_{Gi}, which must equal the recombination current I_R supported by the forward-biased source-body junction, was measured by integrating the hole current flowing out of the drain junction; the results are plotted versus V_{BS} in Fig. 3.5. For these plots, I_{Gi} was normalized (by multiplying by 2 for device C, and by 1/1.4 for device A) to exclude the dependence of the I_R-V_{BS} relation on the cross section (Wt_b) of the body-source junction. We can see that the I_{Gi} (= I_R) versus V_{BS} curve of the thickest device (device A) shows a normal diode characteristic with $n \cong 2$ at lower V_{BS} and $n \cong 1$ at higher V_{BS}. In the thinnest device, however, $n \cong 1$ even at very low V_{BS}. These simulation results reveal then that in the thin, fully depleted device, unlike a normal diode, the source junction space-charge region recombination is negligible. This effect, analogous to the modulation of recombination in a gated diode, is due to the vertical field separating holes and electrons near the junction. The predominant recombination thus occurs in the quasi-neutral source region (with $n = 1$) away from the junction for all values of V_{BS}, which must hence be higher than that in the thicker device to support I_{Gi}.

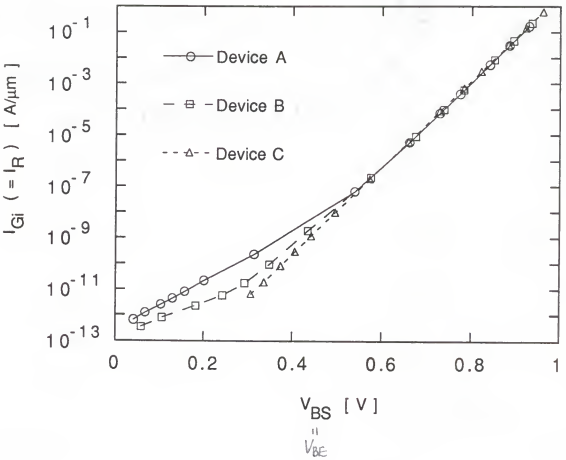


Fig. 3.5 Recombination current as a function of V_{BS}, extracted from simulations in Fig. 3.2.

How then can the disappearance of the kink in the thinner (fully depleted) devices be explained? The explanation is simply that V_{Tf} of the fully depleted device is not sensitive to the body bias V_{BS}, whereas that of the thicker bulk-like device is. In the latter device, V_{BS} effectively reduces the front-surface band bending required for strong inversion (inverse body effect). This reduces V_{Tf} by diminishing the depletion charge that must be supported by the gate. However in the fully depleted device, the depletion (body) charge is fixed, and hence V_{Tf} is independent of V_{BS} [Lim85]. This independence prevails so long as the (injected) net carrier charge in the body remains insignificant.

3.2.2 Parasitic BJT Effects

Since the V_{BS} induced in fully depleted devices is substantial, and even higher than that in thicker devices (see Fig. 3.4), a significant BJT action can occur [Mck89], even though no kink is discernible. Electrons are injected into the body (base) from the source (emitter) and are collected by the drain (collector). This added drain current augments the impact ionization, which in turn drives the body harder, thereby causing a regenerative action. The result is a premature breakdown [You89] (common-emitter BV_{CE0}) or a latch [Che88] (loss of gate control), which portends stand-by-current problems in SOI CMOS circuits. The simulation in Fig. 3.2 shows the breakdown. It should be noted that the

breakdown voltage is well below that of the isolated drain-body junction, and that it is not predicted when the impact ionization in the simulator is turned off. This latter observation means that punchthrough is not causing the excessive conduction in Fig. 3.2.

To gain more insight regarding control of the BJT effects, we analyzed dependences of breakdown voltage on device parameters, L, t_b, N_A, and τ_0 in (3.1). Simulated I_{DS}-V_{DS} characteristics of fully depleted MOSFETs (including devices B and C in Fig. 3.2) with different parametric values at fixed $(V_{Gfs}-V_{Tf})$ = 2 V are plotted in Fig. 3.6. To adequately explain the breakdown voltages in Fig. 3.6, we must consider the parametric dependences of the impact ionization as well as the BJT action, since BV_{CEO} depends on both mechanisms. To see this, we note that (see Fig. 3.1)

$$I_{Gi} = (M - 1)(I_{cf} + I_T) \tag{3.3}$$

where I_{Gi} is the generation current due to impact ionization, M is the multiplication factor, I_{cf} is the MOSFET (front) channel current, and I_T is the BJT base transport (collector) current, which we can write as

$$I_T = \beta I_{Gi} \quad . \tag{3.4}$$

Combining (3.3) and (3.4) yields

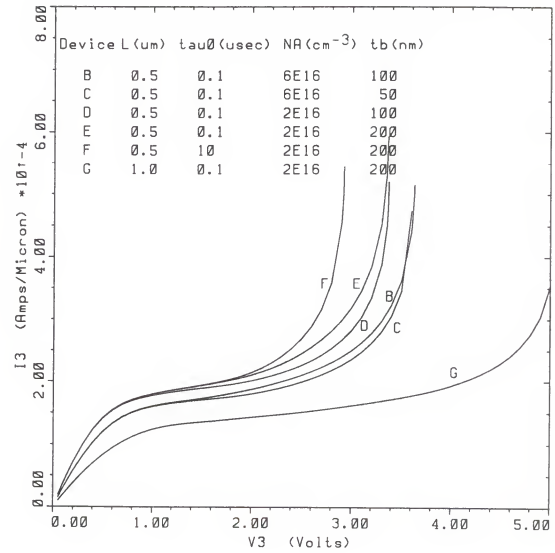


Fig. 3.6 PISCES-simulated I_{DS}-V_{DS} characteristics with (V_{Gfs}-V_{Tf}) = 2 V for a variety of fully depleted devices. In the figure, V3 and I3 denote V_{DS} and I_{DS} respectively.

$$I_{DS} = M(I_{cf} + I_T) = \frac{MI_{cf}}{1 - \beta(M-1)} \quad , \tag{3.5}$$

which indicates that the breakdown occurs where $\beta(M-1) \approx 1$. We stress however that, as we will demonstrate, both $(M-1)$ and β depend strongly on the bias condition, and optimal design will be influenced by these dependences. $(M-1)$ and β can be characterized from device simulations, whereas it is virtually impossible to do so experimentally for floating-body devices.

From the PISCES output files of the simulations in Fig. 3.6, we calculated $(M-1) = I_{Gi}/(I_{DS}-I_{Gi})$ at different bias points. This calculation involved evaluating I_{Gi} in (3.3) by integrating the hole current flowing out of the drain junction as we did for Fig. 3.5. The results are plotted in Fig. 3.7. Notice that the extracted $(M-1) \ll 1$; the impact ionization is weak, which is characteristics of BV_{CEO} breakdown. Notice also the strong dependence of $(M-1)$ on V_{DS}, which strengthens near the breakdown. To first order, $(M-1) \propto \exp(-\beta_0/E)$ with the drain field $E \propto V_{DS}$ [Elm77]; but as the BJT is activated, E is modulated due to electrons constituting I_T. Under high injection conditions in the body (BJT base), the electron charge increases the negative (ionized-acceptor) charge in the drain-junction space-charge region, thereby shrinking it and increasing E, and hence accelerating the increase of $(M-1)$ with V_{DS}. This explanation

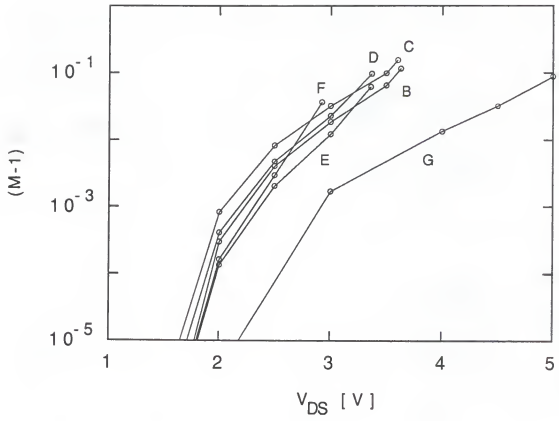


Fig. 3.7 Impact-ionization multiplication factor extracted from simulations in Fig. 3.6.

is consistent with variations in the drain potential predicted by the simulations.

We also calculated β from the simulation results. This calculation, based on (3.5), involved estimating I_{cf} by simulating the device with the impact ionization turned off. The results are plotted in Fig. 3.8. Note that β decreases dramatically with increasing V_{DS}. This is explained by the high-injection condition in the body (base) corresponding to V_{BS}. As discussed previously, the predominant recombination (I_T/β) occurs in the (lightly injected) source, varying as $\exp(V_{BS}/V_{th})$, whereas $I_T \propto \exp(V_{BS}/2V_{th})$ since $p \approx n$ and $pn = n_i^2\exp(V_{BS}/V_{th})$ in the (highly injected) body near the source junction. Indeed the device simulations show $\beta \propto \exp(-V_{BS}/2V_{th})$ approximately as we can see in Fig. 3.9, where we plot β of the devices in Fig. 3.6 as a function of V_{BS} defined by (3.2). The solid line shows the slope for $\beta \propto \exp(-V_{BS}/2V_{th})$.

Now, with reference to Figs. 3.7 and 3.8, consider the parametric dependences of the breakdown voltage reflected by the simulations in Fig. 3.6.

1) Dependence on L:

BV_{CEO} decreases with decreasing L (see devices E and G in Fig. 3.6). The dependence, which is strong for submicron devices, is due to both a larger (M-1) and a higher β in a short-channel device. (M-1) is larger because of carrier-velocity saturation in the channel, which reduces $V_{DS(sat)}$ and

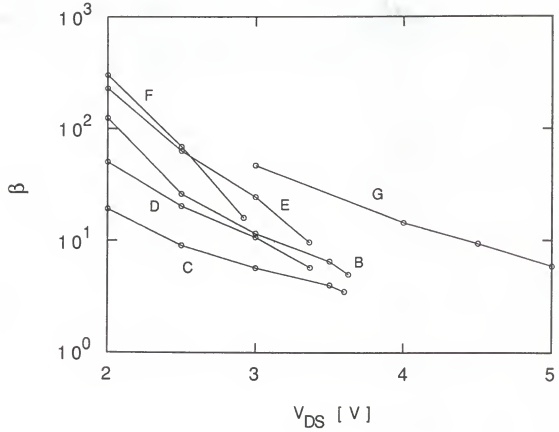


Fig. 3.8 BJT current gain extracted from simulations in Fig. 3.6.

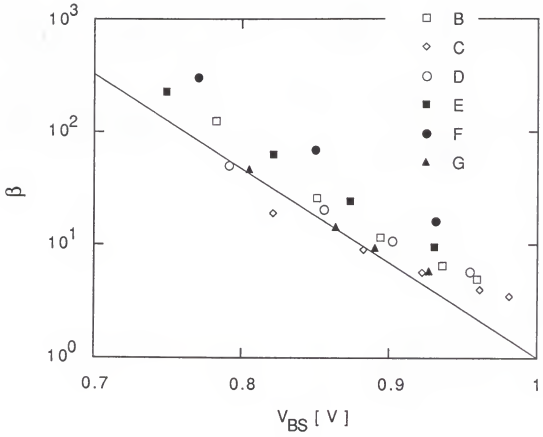


Fig. 3.9 BJT current gain as a function of V_{BS}, extracted from simulations in Fig. 3.6. The solid line shows the slope for $\beta \propto \exp(-V_{BS}/2V_{th})$.

increases E in the drain region of the short-channel MOSFET [Vee88b]. β is higher because of the narrower base width ($\approx$L), which enables higher I_T ($\propto$ 1/L) for a given V_{BS}.

2) Dependence on t_b:

BV_{CEO} is not strongly dependent on t_b (see devices B and C, and D and E in Fig. 3.6). This insensitivity is due to the increase in (M-1), as discussed in Chapter 2, being compensated by a decrease in β as t_b is thinned, as well as being modulated near breakdown as discussed with reference to Fig. 3.7. β decreases because I_{Gi} is higher, and hence V_{BS} is higher in support of the equalizing recombination current which obtains from a smaller volume ($\propto t_b$). The higher V_{BS} means a higher injection level, and hence a lower β commensurate with the discussion of Fig. 3.8.

3) Dependence on N_A:

BV_{CEO} increases with increasing N_A (see devices B and D in Fig. 3.6). This dependence is moderate, and is due to less drain-field modulation (discussed previously in reference to Fig. 3.7) in the higher-doped device, as well as lower carrier mobility in the channel. The lower mobility tends to defer velocity saturation and hence increase $V_{DS(sat)}$, which reduces (M-1) [Vee88b]. The mobility is lower because of more ionized-impurity scattering and increased surface scattering due to higher transverse field. However the low-field mobility assumed in PISCES for the channel is based on bulk-

silicon mobilities, and consequently the N_A dependence predicted may be exaggerated.

4) Dependence on τ_0:

BV_{CEO} increases with decreasing τ_0 (see devices E and F in Fig. 3.6). This dependence however is not as significant as we might surmise because of the highly nonlinear dependences of (M-1) and β on injection level (see Figs. 3.7 and 3.8). For shorter τ_0, the recombination equalizing I_{Gi} is supported by a lower V_{BS}. Thus I_T is smaller and β is lower. However the lower V_{BS} tends to defer the high injection which reduces β as we have discussed, but which also cause the sharp increase in (M-1) due to the drain-field modulation. Furthermore since the predominant recombination occurs in the highly doped source, it is governed in part by the fundamental band-band Auger process [Foss83], independent of τ_0. The net result then is only a moderate increase in BV_{CEO}. We note that a more dramatic decrease in τ_0, effected for example by intentional lifetime killing, could produce a more significant increase in BV_{CEO}, but at the expense of prohibitive leakage current.

The BV_{CEO} breakdown of the SOI MOSFET/BJT structure discussed to this point is driven by (front) channel current in combination with the drain-source voltage. In an actual SOI CMOS circuit, for example the CMOS inverter, this particular activation of the BJT is in fact beneficial. The BJT conduction in the n-channel MOSFET would speed the

discharging of the load and the pull-down of the inverter output voltage, V_{DS}. There would be no possibility of a sustained latch of the BJT because V_{DS} is lowered (toward zero) by the conduction.

The real BJT-induced problem in SOI CMOS is the possibility of a latch when the MOSFET is supposed to be off, i.e., when $V_{GfS} < V_{Tf}$, and there is no significant channel, and V_{DS} is high (= V_{DD}). Such a latch, viz., the triggering of the open-base BJT into the BV_{CEO} mode of conduction, could occur if significant impact ionization is initiated by back-channel leakage current, or if the BJT is driven by significant thermal-generation leakage current or radiation-induced current. The effect on the circuit would not be a loss of the logic state, but excess stand-by current to support it. The implied power consumption is prohibitive.

To gain more insight concerning this latch, we simulated the dc subthreshold latch which has been previously reported [Che88], but has not been adequately analyzed. In Fig. 3.10 we plot simulated $\log(I_{DS})$-V_{GfS} characteristics of device D in Fig. 3.6 for V_{DS} = 2.2 V. Curves for both forward and reverse scans of V_{GfS} are shown, with and without the impact ionization in PISCES turned on. Note that with the impact ionization turned off, the characteristics are normal. However with the impact ionization on, the device cannot be turned off. There is a complete loss of gate control in the reverse scan due to the activation of the BJT. As described

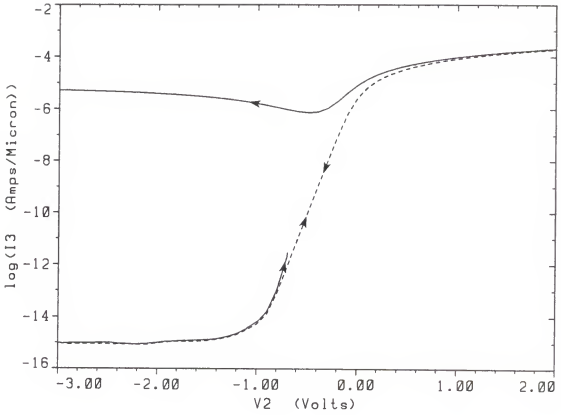


Fig. 3.10 PISCES-simulated $\log(I_{DS})$-V_{GfS} characteristics at V_{DS} = 2.2 V, with (solid curve) and without (dashed curve) impact ionization, for device D in Fig. 3.6. Both forward- and reverse-V_{GfS} scans are indicated. In the figure, V2 and I3 denote V_{GfS} and I_{DS} respectively.

in our discussion of the BV_{CEO} effect, the BJT is activated by channel current-induced impact ionization in the on-state, and remains on even as V_{GfS} drops below V_{Tf}. (This reverse-scan latch is predicted by PISCES because the numerical simulation at each bias point uses the previous solution as an initial guess in the iterative derivation of the current solution.) This particular latch is not necessarily problematical in SOI CMOS for the same reason that the BV_{CEO} breakdown (Fig. 3.6) is not. In the forward scan in Fig. 3.10, the BJT activation does not occur until sufficient (weak-inversion) channel current flows. (This latch is indicated in the PISCES simulation by no convergence, caused by the discontinuity in I_{DS}.) This subthreshold I_{cf}-induced latch is not problematical in CMOS either.

However for higher V_{DS} = 3 V as in Fig. 3.11, a latch can occur in the forward-V_{GfS} scan even when there is no (front) channel, and this does portend a real problem in SOI CMOS circuits. (This latch is predicted with PISCES by first ramping V_{DS} up to 3 V with V_{GfS} = -3 V, and then increasing V_{GfS}. In this case, the device is latched before V_{GfS} is increased.) Why does this latch occur, and what does it imply about SOI CMOS latch? At low V_{GfS} (« V_{Tf}), there is no channel current, yet the BJT is activated and its current induces the impact ionization to cause the regenerative action. This means that substantial thermal-generation (I_{Gt}) or impact ionization caused by back-channel current (I_{cb}) initially

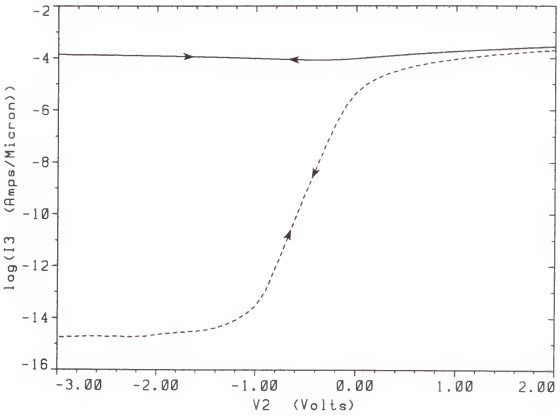


Fig. 3.11 PISCES-simulated $\log(I_{DS})$-V_{GfS} characteristics at V_{DS} = 3 V, with (solid curve) and without (dashed curve) impact ionization, for device D in Fig. 3.6. Both forward- and reverse-V_{GfS} scans are indicated. In the figure, V2 and I3 denote V_{GfS} and I_{DS} respectively.

drives the BJT, and ultimately I_T induces sufficient impact ionization to latch the device. The origin of I_{Gt} is SRH generation in the drain junction space-charge region, governed by the lifetime in (3.1). The origin of I_{cb} is drain-induced barrier lowering (DIBL) at the back surface, which depends on V_{DS} and V_{GfS}.

If the leakage current, comprising I_{Gt} and/or I_{cb}, is high enough, the latch condition can be reached even though there is no front-channel current. To see this, rewrite (3.4) for this case as

$$I_T = \beta(I_{Gi} + I_{Gt}) \tag{3.6}$$

where now

$$I_{Gi} = (M - 1)(I_T + I_{cb}) \quad . \tag{3.7}$$

Combining (3.6) and (3.7) yields

$$I_{DS} = M(I_T + I_{cb}) + I_{Gt} = \frac{(\beta + 1)I_{Gt} + MI_{cb}}{1 - \beta(M-1)} \quad . \tag{3.8}$$

Note that the denominator in (3.8) is identical to that in (3.5), indicating the same condition for off-state latch as for the breakdown: $\beta(M-1) \approx 1$. The key to this latch is that $(M-1)$ is high in the subthreshold region since $V_{DS(sat)} \approx 0$ and the drain field is very high [Vee88b]. Thus I_{Gt} or I_{cb} need

only be high enough to drive V_{BS} up to a point where $\beta \approx 1/(M-1)$, which might not be much higher than unity for $V_{DS} = V_{DD}$.

Evidently, subject to some uncertainty in the PISCES solutions, β can be sufficiently high in the fully depleted SOI MOSFET to support the off-state latch characterized in (3.8), even when the BJT is activated by low leakage current. This is surprising since in more conventional BJTs, β falls off drastically at low current (due to emitter-base junction space-charge region recombination.) Crudely, for $\tau_0 = 100$ ns as in the PISCES simulations of Fig. 3.11, we would expect $\beta \approx 10^{-2}\exp(V_{BS}/2V_{th})$, which is much less than unity for V_{BS} defined by the generation current simulated. However as we discussed previously, the junction space-charge region recombination tends to be suppressed in the fully depleted device due to the gate-controlled field, and hence V_{BS} and β are higher than anticipated.

3.3 Optimal Design Considerations

The off-state leakage current-induced latch must be avoided in SOI CMOS circuits. Based on (3.8) and on the insight afforded by the parametric analyses in Section 3.2.2, we discuss here device design to control this latch. As is evident in (3.8), both (bias-dependent) β and (M-1) must be considered in the optimal design. Thickening t_b will reduce (M-1) significantly. (It will also exacerbate the short-channel effects [Vee89], thus implying a design tradeoff.)

The benefit thereby afforded with regard to the off-state latch will be more substantive than that indicated by the breakdown discussion in Section 3.2.2 because the high-injection effects on β, which diminish the sensitivity of BV_{CEO} to t_b, will not materialize prior to the latch.

With regard to reducing β, we must maximize the recombination current in the quasi-neutral source (emitter) region, which is the dominant component in fully depleted devices as we discussed in Section 3.2.1 with reference to Fig. 3.5. Thus for the source structure depicted in Fig. 3.1,

$$I_R \equiv I_{R0}\exp\left(\frac{V_{BS}}{V_{th}}\right) \tag{3.9}$$

where I_{R0} follows from the solution of the two-dimensional hole transport in the heavily doped source region. Since I_R equals the total generation current, I_{R0} in (3.9) defines V_{BS}, which in turn drives I_T exponentially. Hence to reduce β, I_{R0} should be maximized, which would minimize V_{BS} for a given generation current.

For physical insight, we analytically express

$$I_{R0} \equiv \frac{q\,A(t_b)\,n_i^2}{N_{D(eff)}}\,\frac{V_{th}\,\mu_p}{L_S} \quad , \tag{3.10}$$

which is a semi-empirical extension of a one-dimensional model [Fossu81] of hole transport in n^+ silicon. In (3.10), the area A depends on t_b ($\approx Wt_b$), but not necessarily linearly

due to the two-dimensional nature of the hole flow in the source, which we characterize by the effective (diffusion) length L_S. L_S depends on the geometry of the source as well as the doping and hole lifetime in it. $N_{D(eff)}$ is the effective doping density [Fossu81], which is less than the actual doping N_{DS} because of bandgap narrowing in the n^+ source. The hole mobility μ_p decreases with increasing N_{DS}. From (3.10) we infer that the most effective way to increase I_{R0} is to decrease $N_{D(eff)}$ and/or to reduce L_S.

In essence, $N_{D(eff)}$ is defined [Fossu81] by

$$N_{D(eff)} = N_{DS} \exp(-\frac{\Delta E_g}{kT}) \tag{3.11}$$

where ΔE_g is the (effective) bandgap narrowing (which can be affected by majority-electron degeneracy as well as the modulation in density of quantum states caused by heavy doping). The relation in (3.11) between $N_{D(eff)}$ and N_{DS}, which is assumed to equal the electron density, reflects the effects of hole-electron mass action and the fact that the pn-product increases with decreasing bandgap. The nonlinear dependence of ΔE_g on N_{DS}, and the fact that it is not significant unless $N_{DS} > \approx 10^{18}$ cm^{-3} result in only a weak dependence of $N_{D(eff)}$ on N_{DS} for $N_{DS} > 10^{18}$ cm^{-3}, and $N_{D(eff)} \cong N_{DS}$ for $N_{DS} < 10^{18}$ cm^{-3}. Thus it will be necessary to reduce N_{DS} below 10^{18} cm^{-3} to substantially increase I_{R0} in (3.10). Physically, lowering $N_{D(eff)}$ increases the hole density in the

quasi-neutral source region for a given V_{BS}. This tends to increase the recombination rate, so long as the injected holes are in close proximity to high densities of recombination centers; that is, so long as L_S in (3.10) is sufficiently short.

This insight then suggests that I_{R0} can be maximized by bringing the high-recombination ohmic contact close to the body-source junction, and significantly reducing the source doping. This design however would not be compatible with technology for two reasons. First, high doping ($>10^{19}$ cm^{-3}) is needed to ensure good ohmic contact. Second, lithography limits the minimum separation between the source contact and the junction in Fig. 3.1. A similar enhancement of I_{R0} however can be achieved by using a lightly doped source (LDS) with a shallow n^+ region near the contact. The low doping in the LDS enables high hole injection extending to the contiguous n^+ region, and the ohmic contact there tends to minimize L_S. We also note that the LDS design must be compatible with the LDD design since the two lightly doped regions should be identical to ensure the viability of the technology, which requires a symmetry.

We show in Fig. 3.12 simulated subthreshold characteristics of device D of Fig. 3.11, but now with a lower-doped source: $N_{DS} = 10^{17}$ cm^{-3}, with a highly doped n^+ region at the contact, and the distance between the n^+ region and the body-source junction was equal to about 0.2 μm. Note

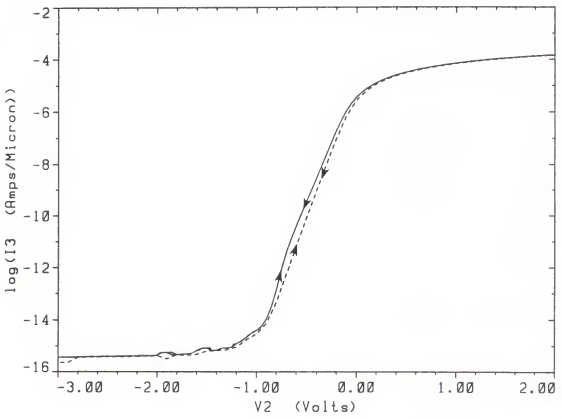


Fig. 3.12 PISCES-simulated log(I_{DS})-V_{GfS} characteristics at V_{DS} = 3 V, with (solid curve) and without (dashed curve) impact ionization, for device D in Fig. 3.11, but now with a lower-doped source: $N_{DS} = 10^{17}$ cm^{-3}. Both forward- and reverse-V_{GfS} scans are indicated. In the figure, V2 and I3 denote V_{GfS} and I_{DS} respectively.

in Fig. 3.12 that the latch has been suppressed by the LDS. A slight body effect caused by the impact-ionization charging [Fossu87] is noticeable. For more insight, we show in Fig. 3.13 the simulated off-state I_{DS} with V_{GfS} = -3 V as a function of V_{DS} for both the original (D) and LDS (D^*) versions of the device. Notice, commensurate with the subthreshold characteristics in Figs. 3.11 and 3.12, the significant increase in the value of V_{DS} required to trigger the latch in the LDS device. (Another simulation shows that the isolated drain-body junction breakdown voltage, with V_{GfS} = -3 V, is >8 V.) The characteristics in Fig. 3.13 typify common-emitter, open-base BJT breakdowns. The onset of the latch is triggered by (low) leakage current, and the snap-back (to BV_{CEO}) occurs because of the strong injection-level dependences of (M-1) and β. The forward-V_{GfS}-scan latch, which is problematical in SOI CMOS circuits, is governed by the latch onset which is substantively higher than the snap-back (holding [Mck89]) voltage. Note that the simulated characteristic of device D in Fig. 3.13, showing two stable states (off and latched) at V_{DS} = 2.2 V and only one (latched) at V_{DS} = 3 V, reflects why, at V_{GfS} = -3 V, only reverse-scan latch occurs in Fig. 3.10 but both forward- and reverse-scan latches occur in Fig. 3.11.

Closer examination of the simulations of devices D and D^* in Fig. 3.13 reveals interestingly that lowering N_{DS} not only reduced β but also suppressed the back-channel DIBL

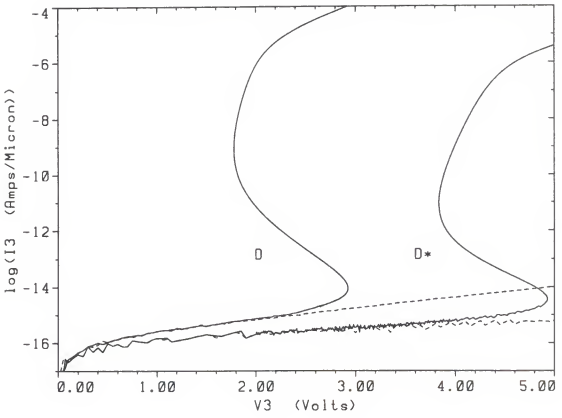


Fig. 3.13 PISCES-simulated off-state $\log(I_{DS})-V_{DS}$ characteristics of the two versions of device D at V_{GfS} = -3 V with (solid curve) and without (dashed curve) impact ionization. The LDS device (D*) latches at significantly higher V_{DS}. In the figure, V3 and I3 denote V_{DS} and I_{DS} respectively.

leakage current (I_{cb} in (3.8)), which is the predominant leakage component in device D. This suppression is due to the lightly doped source reducing the lateral field encroachment in the film body, thereby limiting the two-dimensional effects. Hence additional design tradeoffs to control the DIBL (and other short-channel effects) are implied.

Finally we show in Fig. 3.14 the simulated on-state I_{DS}-V_{DS} characteristics of devices D and D* with $(V_{GfS}-V_{Tf}) = 2$ V. Commensurate with the suppression of the off-state latch, but not in direct proportion because of the bias-dependences of (M-1) and β, the LDS device (D*) shows a much higher breakdown voltage. The simulation results further confirm that β has been reduced by lowering the source doping, and they show that (M-1) has been reduced also (because of the effect of the LDS resistance on the saturation characteristics of the short-channel MOSFET).

We stress that the PISCES simulations are not necessarily precise, but they reflect true trends. Furthermore the simulations did not include an LDD. In an optimal design, an LDD would be included to restrict the drain field, and hence control (M-1). Our analysis suggests that an LDS also be included to control β, and to suppress DIBL, which is most significant at the back surface. Then with t_b and N_A chosen to effect the tradeoffs regarding short-channel effects [Vee89] (e.g., the DIBL) and hot-carrier-defined reliability [Hu85], the LDD/LDS SOI MOSFET can be

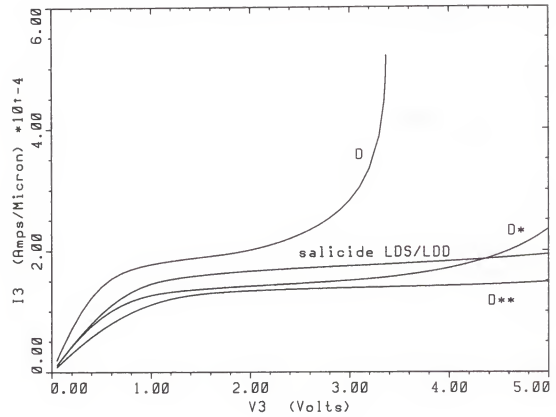


Fig. 3.14 PISCES-simulated I_{DS}-V_{DS} characteristics of the three versions of device D at (V_{Gfs}-V_{Tf}) = 2 V. D^* is the LDS device. D^{**} is the LDS/LDD device including an indentical LDD region. The characteristic of the salicide-contact LDS/LDD device with higher LDS/LDD doping is also included. In the figure, V3 and I3 denote V_{DS} and I_{DS} respectively.

suitable and in fact desirable for submicron CMOS applications. With the LDS, there is an obvious tradeoff involving drive current (limited by the source resistance as indicated in Fig. 3.14) and the off-state latch for the optimal design. However design optimization seems plausible.

With the study of hot-carrier-defined reliability in Chapter 2, our analysis herein suggests that a moderately thin SOI technology with an LDD and an LDS is advantageous as well as viable for submicron CMOS applications, perhaps even with a 5-V supply voltage. In fact, additional simulations of device D^{*}, including an LDD identical to the LDS, show that both the breakdown in Fig. 3.14 and the onset of the off-state latch in Fig. 3.13 are increased to >7 V, with no appreciable additional reduction in drive-current capability. These results are reflected by the simulated LDS/LDD device D^{**} characteristic in Fig. 3.14.

As we will discuss in Chapter 4, the characterization of I_{R0} in the LDS device we simulated is more complex than (3.10), which assumes a uniform source doping. The general model is defined by the hole transport in both the n^{+} and n^{-} regions. The device design optimization will require a comprehensive physical analysis of the transport in the LDS; note for example that the electric field associated with the ohmic drop actually enhances recombination in the source. The design will also have to account for an identical LDD, which

must be part of the optimal device for both technological and electrical reasons.

Perhaps to lend some flexibility to the design optimization of the LDS/LDD SOI MOSFET, we consider the incorporation of self-aligned silicide (salicide) contacts [Gal90], which should be used ultimately in VLSI to minimize contact resistance. Shown in Fig. 3.15 is an LDS structure with a salicide source contact. In such a structure, the n^+ layer separating the LDS from the silicide can be quite thin ($\approx$ 20 nm), and the silicide-silicon interface is a high-recombination surface like an ohmic contact. The PISCES simulated I_{DS}-V_{DS} characteristic of the device D, but with this source (and identical LDD drain) structure (with the silicide modeled as an ohmic contact) is included in Fig. 3.14. Both the LDS and LDD lengths were about 0.2 μm, but the doping was increased to 3×10^{17} cm^{-3} to illustrate afforded flexibility and validity in the required design optimization. The n^+ layer thickness T_{n^+} was about 20 nm. Note that, compared with the LDS device (D^*), the drive current is increased due to the higher LDS doping, and the breakdown voltage is increased due to incorporation of the LDD. An additional simulation shows that the off-state latch voltage of this salicide LDS/LDD device is about 6.5 V.

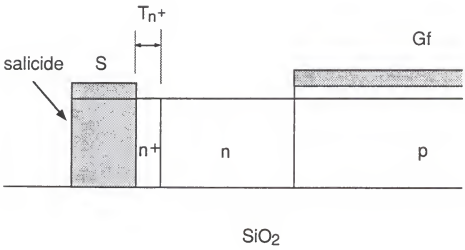


Fig. 3.15 Salicide-contacted source structure of n-channel SOI MOSFET with LDS.

3.4 Summary

Copious PISCES simulations of fully depleted floating-body submicron SOI MOSFETs revealed significant body charging (viz, V_{BS}), even though no kink was discernible. Commensurate parasitic BJT-induced breakdown and latch phenomena were predicted, in both the on- and off-states. These phenomena were analyzed and characterized in terms of the impact-ionization multiplication factor (M-1) and the BJT current gain β. Both (M-1) and β are highly nonlinear; they were extracted from the simulations to gain physical insight concerning the BJT-induced effects since it is virtually impossible to do so by measurements. We believe that this is the first successful try in characterizing the parasitic BJT in floating-body SOI MOSFETs. It was found that high injection in the body, and associated drain-field modulation significantly affect (M-1) and β, and hence the breakdown voltage and the latch-onset conditions.

Parametric dependences noted from the simulations were used to gain physical insight for design optimization of fully depleted submicron SOI MOSFETs. The BV_{CEO} breakdown and the reverse-V_{GFS}-scan subthreshold latch do not seem to be harmful to SOI CMOS circuit performance, but the off-state latch in the forward scan does reflect a stand-by-current problem (prohibitive power consumption). This off-state latch is induced when the parasitic BJT is activated by thermal-generation leakage current and/or impact-ionization current

caused by back-surface DIBL leakage current. A lightly doped source was shown to increase the latch voltage by reducing β. The technical aspect of the LDS design was discussed and the use of contemporary self-aligned silicide-contact technology was suggested for the LDS design. Even though a tradeoff involving drive current is implied, the LDS structure, including an LDD to help control (M-1), seems to be a viable approach to optimizing and exploiting the advantages of fully depleted submicron SOI CMOS.

We note that, with reference to the discussions in Chapter 2, using a moderately, but not extremely thin film is advantageous for increasing the long-term device lifetime. However, as the channel length is scaled to the deep-submicron range, the upper limit of film thickness will be defined mainly by the short-channel effects, including the increase of leakage currents due to back-channel DIBL and/or punchthrough. These leakage currents can actually trigger the parasitic BJT action discussed in this chapter, as well as disable the effective MOSFET operation.

CHAPTER 4
A COMPREHENSIVE MODEL FOR THE FULLY DEPLETED SOI MOSFET

4.1 Introduction

The SOI MOSFET model [Vee88b] used for the simulations discussed in Chapter 2, while useful for the study of hot-carrier-induced degradation, is inadequate for CAD based on contemporary SOI CMOS technology involving fully depleted, floating-body devices. In this chapter, we substantively extend the model based on comprehensive analysis of (ambipolar) carrier transport in extrinsic (parasitic) as well as intrinsic parts of the advanced thin-film SOI MOSFET structure. The modeling is done for ultimate implementation into the device/circuit simulator SOISPICE [Fit89], which is discussed in the next chapter.

Figure 4.1 is a representative cross-sectional view of the contemporary thin-film n-channel SOI MOSFET. The n^- regions represent a lightly doped source (LDS) and a lightly doped drain (LDD). We assume this basic structure for the model derivation in this chapter.

The model extension includes physical accountings for subthreshold currents at both the front and back surfaces, parasitic BJT current, recombination current at the source-

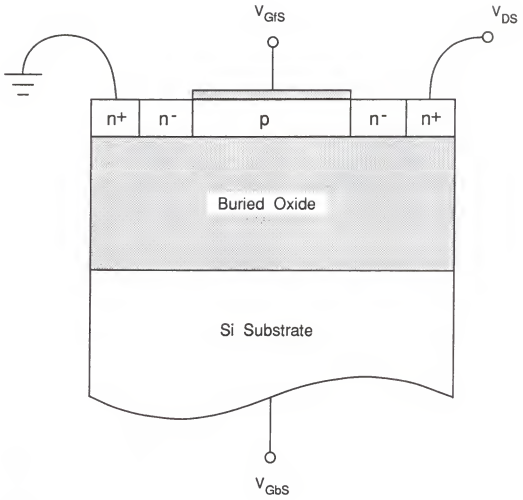


Fig. 4.1 A cross-sectional view of the contemporary thin-film n-channel SOI MOSFET including an LDS and an LDD.

body junction, effects of LDS and LDD regions, and thermal generation leakage current in the fully depleted SOI MOSFET. The underlying analyses are aided by physical insights gained from the studies in Chapters 2 and 3. Mobility and carrier lifetime, which are used throughout the model derivation, are characterized empirically based on published work. We note that the model is derived for an n-channel MOSFET, but it is applicable as well to a p-channel device with appropriate changes in notation.

The new analyses are done with direct linkage to the previously developed model [Vee88b], and hence they effectively produce a comprehensive and contemporary version. We assume full depletion of the film body for the entire gate-bias range. Implicitly then the film thickness (t_b) is assumed to be less than the maximum depletion-region width ($x_{d(max)}$). As discussed in Chapter 2, back-surface accumulation of the depleted film (TFA) is not beneficial, and is not likely to occur under normal bias conditions since TFA is possible only with unusually high back-gate bias. Therefore the models are derived with the assumption that TFA will not obtain.

4.2 Subthreshold Current Model

In fully depleted SOI CMOS, the dominant leakage can be attributed to back-channel subthreshold current since the substrate is generally grounded to ensure full depletion in

both the n- and p-channel MOSFETs. In short-channel devices, this leakage increases with V_{DS} due to drain-induced barrier lowering (DIBL), which is the weak-inversion counterpart to DICE [Vee88b] in strong inversion. Figure 4.2 shows measured subthreshold leakage current, reflecting the back-channel DIBL problem in a fully depleted n-channel MOSFET. This leakage, if unconstrained, will cause a stand-by power consumption problem in CMOS circuits, and it can trigger the BJT-related latch as we discussed in Chapter 3. An accounting for this current component is therefore essential in any practical device/circuit simulator for advanced SOI. The model for the front-channel subthreshold current with DIBL is also included in this work to render SOISPICE more robust in a sense that it can be useful for simulation of circuits using a low power-supply voltage.

4.2.1 Front-Channel Subthreshold Current

With the diffusion-only approximation [Sze81], the front-channel subthreshold (weak-inversion) current is expressed as

$$I_{cf(weak)} = W\, V_{th}\, \bar{\mu}_{nf}\, \frac{\partial Q_{cf}(y)}{\partial y} \qquad (4.1)$$

where W is the channel width, V_{th} is the thermal voltage kT/q, $\bar{\mu}_{nf}$ is an average front-channel electron mobility (described later), and $Q_{cf}(y)$ is the front-channel weak-inversion

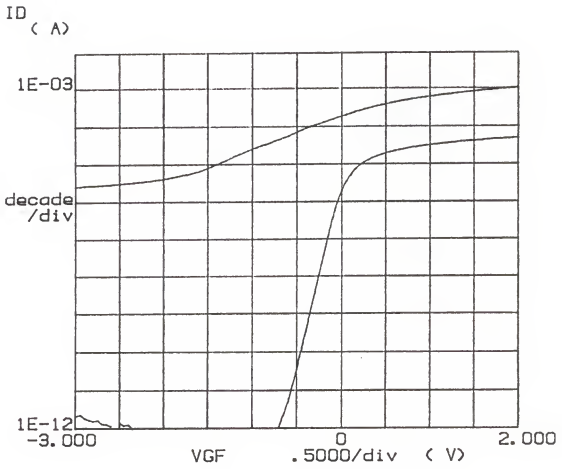


Fig. 4.2 Measured subthreshold characteristics of a fully depleted n-channel MOSFET, as a function of V_{DS}, with V_{BS} = 0 V and V_{GbS} = -5 V; V_{DS} = 0.05 V for the lower curve, and V_{DS} = 5 V for the upper curve. The device measured has W/L = 3.6 μm/0.8 μm, t_b = 0.28 μm, and $N_A \equiv 8 \times 10^{15}$ cm^{-3}.

electron charge density. Here we implicitly assume $\bar{\mu}_{nf}$ is not a function of y since the longitudinal field is low in the weakly inverted channel. Integrating $I_{cf(weak)}$ from the source (y = 0) to the drain (y = L) yields

$$I_{cf(weak)} = \frac{W}{L} V_{th} \bar{\mu}_{nf} [Q_{cf}(L) - Q_{cf}(0)] \quad . \tag{4.2}$$

Since the variation in electrostatic potential (band bending) across the inversion-layer thickness $X_i(y)$ is only a few (m) times V_{th}, $Q_{cf}(y)$ can be written as

$$\begin{aligned} -Q_{cf}(y) &= q \int_0^{X_i(y)} n(x,y)\, dx \\ &= q \int_{\psi_{sf}}^{\psi_{sf}-mV_{th}} \frac{n(\psi)}{\partial\psi/\partial x}\, d\psi \\ &\cong q \frac{1}{\bar{E}_{xf}} \int_{\psi_{sf}-mV_{th}}^{\psi_{sf}} n(\psi)\, d\psi \end{aligned} \tag{4.3}$$

where ψ_{sf} is the front-surface band bending and n is the channel electron density. $\bar{E}_{xf}$ is an average transverse electric field felt by channel electrons, which can be expressed in a simple form for the weak-inversion case. For the condition that Q_{cf} is small, Eq. (16) in [Vee88b] is simplified, through manipulation of Eqs. (2.16), (2.17), and (2.18) in [Vee88a], to

$$\bar{E}_{xf} \cong \frac{\psi_{sf} - \psi_{sb}}{t_b} - \frac{Q_{b(eff)}}{2\varepsilon_s} \tag{4.4}$$

where $Q_{b(eff)}$ is the effective body depletion charge density and ψ_{sb} is the back-surface band bending, which will be derived later. $\bar{\mu}_{nf}$ in (4.2) is defined [Vee88b] by this average field as

$$\bar{\mu}_{nf} = \frac{\mu_{n0}}{1 + \theta \bar{E}_{xf}} \tag{4.5}$$

where μ_{n0} is the low-field mobility and θ is an empirical constant that characterizes the field-effect mobility degradation.

Since [Sze81]

$$n(\psi) = \frac{n_i^2}{N_A} \exp\left(\frac{\psi - V_y}{V_{th}}\right) \tag{4.6}$$

where V_y is the Fermi-potential separation at y due to the applied drain voltage V_{DS}, (4.3) gives

$$-Q_{cf}(y) \cong \frac{q n_i^2}{N_A} \frac{1}{\bar{E}_{xf}} \int_{\psi_{sf}-mV_{th}}^{\psi_{sf}} \exp\left(\frac{\psi - V_y}{V_{th}}\right) d\psi$$

$$\cong \frac{q n_i^2}{N_A} \frac{V_{th}}{\bar{E}_{xf}} \exp\left(\frac{\psi_{sf} - V_y}{V_{th}}\right) . \tag{4.7}$$

Combining (4.2) and (4.7), with $V_y(0) = 0$ and $V_y(L) = V_{DS}$, we get

$$I_{cf(weak)} \cong \frac{W}{L} V_{th}^2 \bar{\mu}_{nf} \frac{qn_i^2}{N_A} \frac{1}{\bar{E}_{xf}} \exp\left(\frac{\psi_{sf}}{V_{th}}\right) \left[1-\exp\left(-\frac{V_{DS}}{V_{th}}\right)\right] . \qquad (4.8)$$

Note that (4.8) implies that the saturation drain voltage $V_{DS(sat)}$ is just a few times V_{th} in subthreshold [Sze81].

In saturation, the length of the channel L_{ef} is less than the gate length L because of channel-length modulation [Vee88b]. In this case, $V_y(L_{ef}) = V_{DS(eff)} \cong V_{DS(sat)}$. For subthreshold based on (4.8), we assume $V_{DS(eff)} \cong 0$, and then the effective channel length L_{ef} [Vee88b] is simplified to

$$L_{ef} \cong L - l_c \sinh^{-1}\left[\frac{\bar{\mu}_{nf} V_{DS}}{2 v_{sat} l_c}\right] . \qquad (4.9)$$

Here v_{sat} is the electron saturated drift velocity, and the characteristic length l_c is given by [Vee88b]

$$l_c = t_b \left[\frac{C_b \beta}{2C_{of}(1+\alpha)}\right]^{1/2} \qquad (4.10)$$

where $\alpha = C_b C_{ob}/(C_b+C_{ob})C_{of}$ and $\beta = 1 + C_b/(C_b+C_{ob})$. The body capacitance C_b is equal to ε_s/t_b, and C_{ob} and C_{of} are the back- and the front-gate oxide capacitances respectively.

To complete the characterization of $I_{cf(weak)}$ in (4.8), we need ψ_{sf} and ψ_{sb} in terms of terminal voltages. To provide a proper linkage to the previously developed strong-inversion model [Vee88b], the front-channel threshold voltage V_{Tf} will be used in the characterization of ψ_{sf}. It is not essential to

do this, but it is an efficient approach since V_{Tf} must be calculated in the model algorithm anyway to determine whether the device is in weak inversion or not.

Neglecting Q_{cf} in subthreshold, we reduce Eq. (2a) in [Vee88b] for $V_{DS} = 0$ to

$$V_{GfS} = V_{FB}^{f} + (1+\frac{C_b}{C_{of}})\psi_{sf0} - \frac{C_b}{C_{of}}\psi_{sb0} - \frac{Q_{b(eff)}}{2C_{of}} \qquad (4.11)$$

where V_{GfS} is the front gate voltage and V_{FB}^{f} is the front-channel flatband voltage. Note that the subscript 0 in (4.11) refers to the solution at $V_{DS} = 0$. By definition $\psi_{sf0} = 2\phi_B$ at threshold, and hence the front-channel threshold voltage V_{Tf} is from (4.11)

$$V_{Tf} = V_{FB}^{f} + (1+\frac{C_b}{C_{of}})2\phi_B - \frac{C_b}{C_{of}}\psi_{sb0}^{*} - \frac{Q_{b(eff)}}{2C_{of}} \qquad (4.12)$$

where ϕ_B is the Fermi potential of the body region and ψ_{sb0}^{*} is the value of ψ_{sb0} when $V_{GfS} = V_{Tf}$. Here $Q_{b(eff)}$ is a weak function of ψ_{sb0} [Vee88b], but the dependence is considered as negligible. ψ_{sb0}^{*} is defined by Eq. (2b) in [Vee88b] with $\psi_{sf0} = 2\phi_B$ and the back-channel charge density $Q_{cb0} = 0$ for fully depleted devices:

$$\psi_{sb0}^{*} = \frac{C_{ob}}{C_{ob}+C_b}\left[V_{GbS} - V_{FB}^{b} + \frac{Q_{b(eff)}}{2C_{ob}} + \frac{C_b}{C_{ob}}2\phi_B\right] \qquad (4.13)$$

where V_{GbS} is the back gate voltage and $V_{FB}{}^{b}$ is the back-channel flatband voltage. Subtracting (4.12) from (4.11), we have

$$V_{GfS} - V_{Tf} = (1+\frac{C_b}{C_{of}})(\psi_{sf0}-2\phi_B) - \frac{C_b}{C_{of}}(\psi_{sb0}-\psi^*_{sb0}) \quad . \tag{4.14}$$

Also subtracting (4.13) from Eq. (2b) in [Vee88b] with Q_{cb} = 0, we have

$$(\psi_{sb0}-\psi^*_{sb0}) = \frac{C_b}{C_{ob}+C_b}(\psi_{sf0}-2\phi_B) \quad . \tag{4.15}$$

Combining (4.14) and (4.15) yields

$$\psi_{sf0} = 2\phi_B + \frac{V_{GfS}-V_{Tf}}{1+\alpha} \quad , \tag{4.16}$$

which is the needed band bending for V_{DS} = 0. Note that (4.16) is valid only for subthreshold ($V_{GfS} \leq V_{Tf}$) conditions.

For V_{DS} > 0 V, DIBL must be considered. In this case, the perturbation by V_{DS} is expressed as [Vee88b],

$$\Delta Q_{cf} = C_{of}(1+\alpha)\Delta\psi_{sf} - \beta\varepsilon_s t_b V_{DS}/L^2 \quad . \tag{4.17}$$

The second term on the right-hand side of (4.17) is a perturbation on the ΔQ_{cf}-$\Delta\psi_{sf}$ relation caused by DIBL, which affects ψ_{sf} and Q_{cf} simultaneously. Even though subthreshold Q_{cf} is an exponential function of ψ_{sf} as in (4.7), we can

easily show quantitatively, using (4.7), that ΔQ_{cf} is negligible compared with $C_{of}(1+\alpha)\Delta\psi_{sf}$ in typical fully depleted devices in weak inversion. Physically this indicates that V_{DS} affects ψ_{sf} relatively more than Q_{cf} for weak inversion (DIBL), whereas the inverse is true for strong inversion (DICE). Neglecting ΔQ_{cf} in (4.17) then, we have

$$\Delta\psi_{sf} = \frac{\beta\varepsilon_{st_b}V_{DS}}{C_{of}(1+\alpha)L^2} \quad . \tag{4.18}$$

The total subthreshold front-surface band bending is the sum of ψ_{sf0} and $\Delta\psi_{sf}$:

$$\psi_{sf} = 2\phi_B + \frac{1}{1+\alpha}\left(V_{GfS} - V_{Tf} + \frac{\beta\varepsilon_{st_b}V_{DS}}{C_{of}L^2}\right) \quad . \tag{4.19}$$

The equations (4.4), (4.5), (4.8), (4.9), (4.10), and (4.19) fully characterize the front-channel subthreshold current when ψ_{sb} in (4.4) is defined in terms of terminal voltages. ψ_{sb}, including $\Delta\psi_{sb}$ due to DIBL, is derived from Eqs. (2b) and (12) in [Vee88b], with $Q_{cb} = 0$, similarly to the derivation of (4.19):

$$\psi_{sb} = \frac{C_{ob}}{C_{ob}+C_b}\left[V_{GbS}-V_{FB}{}^b+\frac{Q_{b(eff)}}{2C_{ob}}\right] + (\beta-1)\left(\psi_{sf}+\frac{t_b{}^2V_{DS}}{L^2}\right) \quad . \tag{4.20}$$

(4.20) can be expressed as a sum of ψ_{sb0} and $\Delta\psi_{sb}$. The resulting $\Delta\psi_{sb}$ is same as (4.18), but with C_{of}, α, and β

replaced by C_{ob}, α^*, and β^* respectively, where $\alpha^* = C_b C_{of}/(C_b+C_{of})C_{ob}$ and $\beta^* = 1 + C_b/(C_b+C_{of})$. We stress that since C_{ob} is typically much smaller than C_{of}, DIBL is more severe at the back surface.

4.2.2 Back-Channel Subthreshold Current

The back-channel subthreshold current $I_{cb(weak)}$ can be derived exactly the same way that $I_{cf(weak)}$ was derived in the previous section. $I_{cb(weak)}$ is written, similarly to (4.8) with appropriate notation changes, as

$$I_{cb(weak)} \equiv \frac{W}{L_{eb}} V_{th}^2 \bar{\mu}_{nb} \frac{qn_i^2}{N_A} \frac{1}{\bar{E}_{xb}} \exp\left(\frac{\psi_{sb}}{V_{th}}\right) \left[1-\exp\left(-\frac{V_{DS}}{V_{th}}\right)\right] . \quad (4.21)$$

Here ψ_{sb} is still given by (4.20). L_{eb}, $\bar{\mu}_{nb}$, and $\bar{E}_{xb}$ are given similarly to the front-channel counterparts as follows:

$$L_{eb} \equiv L - l_{cb} \sinh^{-1}\left[\frac{\bar{\mu}_{nb} V_{DS}}{2 v_{sat} l_{cb}}\right] , \quad (4.22)$$

$$\bar{\mu}_{nb} = \frac{\mu_{n0}}{1 + \theta \bar{E}_{xb}} , \quad (4.23)$$

and

$$\bar{E}_{xb} \equiv \frac{\psi_{sb} - \psi_{sf}}{t_b} - \frac{Q_{b(eff)}}{2\varepsilon_s} , \quad (4.24)$$

where l_{cb} is given, similarly to l_c in (4.10), as

$$I_{cb} = t_b \left[\frac{C_b \beta^*}{2C_{ob}(1+\alpha^*)}\right]^{1/2} \quad . \tag{4.25}$$

The equations (4.19)-(4.25) fully characterize the back-channel subthreshold current.

The condition of strong inversion at the back surface is not modeled in this work since it must be avoided in actual applications. In the model, $I_{cb(weak)}$ in (4.21) is simply limited above the back-channel threshold by a back-channel limiting current which is described in the next section.

4.2.3 Transition to Strong Inversion

Before we discuss the transition to strong inversion, it is an order to briefly review the previous strong-inversion current model [Vee88b]. In the strong-inversion model, the strong-inversion current I_{ST} is assumed to be zero below threshold, and is given by Eq. (20) in [Vee88b] above threshold. This threshold is mathmetically defined by the effective threshold voltage in Eq. (4) of [Vee89], which is different from V_{Tf} due to the DICE effect:

$$V_{Tf(eff)} = V_{Tf} - \frac{\beta \varepsilon_S t_b V_{DS}}{C_{of} L^2} \quad . \tag{4.26}$$

This $V_{Tf(eff)}$ can be effectively used to calculate I_{ST} in [Vee88b] using Eq. (4) in [Vee89] as well as to define the onset of strong inversion. We can see that, at $V_{GfS} = V_{Tf(eff)}$,

ψ_{sf} in (4.19) is just equal to $2\phi_B$, which is the assumed band bending at threshold, and the subthreshold model developed here incorporates well with the previously developed strong-inversion model at threshold.

To ensure a smooth transition from subthreshold (weak inversion) to strong inversion, we may need a model for moderate inversion [Tsi82]. However, to limit the complexity of the model, we rather choose the common approach exemplified in the BSIM MOSFET model [She87], which utilizes a limiting current for the subthreshold current to effect a smooth transition to strong inversion. This idea, which was originated in [Ant82], has been known to give a transition which is adequate for circuit simulation with SPICE2 [Nag75].

The characterizations of $I_{cf(weak)}$ and $I_{cb(weak)}$ given in the previous section are valid only for subthreshold conditions. They extrapolate to values larger than I_{ST} above threshold. Hence we limit them and express the total (front and back) subthreshold current as

$$I_{WK} = \frac{I_{cf(weak)} I_{LIMIT}^{f}}{I_{cf(weak)} + I_{LIMIT}^{f}} + \frac{I_{cb(weak)} I_{LIMIT}^{b}}{I_{cb(weak)} + I_{LIMIT}^{b}} \quad . \tag{4.27}$$

Then the total channel current I_{CH} is given as a linear sum of I_{WK} and I_{ST}, which is defined in our model, following [Vee88b], only for the front channel:

$$I_{CH} = I_{WK} + I_{ST} \quad . \tag{4.28}$$

In (4.27), I^{f}_{LIMIT} and I^{b}_{LIMIT} are given a la [She87] as follows:

$$I^{f}_{LIMIT} = \frac{\bar{\mu}^{*}_{nf} C_{of}}{2} \frac{W}{L^{*}_{ef}} (nV_{th})^2 [1-\exp(-\frac{V_{DS}}{V_{th}})] \tag{4.29}$$

where n is a fitting parameter equal to about 3, and $\bar{\mu}^{*}_{nf}$ and L^{*}_{ef} are given by (4.4), (4.5), (4.9), (4.10), and (4.20) with $\psi_{sf} = 2\phi_B$, emphasizing the fact that the role of the limiting current is important near threshold. Similarly

$$I^{b}_{LIMIT} = \frac{\bar{\mu}^{*}_{nb} C_{ob}}{2} \frac{W}{L^{*}_{eb}} (nV_{th})^2 [1-\exp(-\frac{V_{DS}}{V_{th}})] \tag{4.30}$$

where $\bar{\mu}^{*}_{nb}$ and L^{*}_{eb} are given by (4.22)-(4.25), now with $\psi_{sb} = 2\phi_B$ and, analogous to (4.20),

$$\psi_{sf} = \frac{C_{of}}{C_{of}+C_b} [V_{GfS}-V_{FB}{}^{f}+\frac{Q_{b(eff)}}{2C_{of}}] + (\beta^{*}-1)(2\phi_B+\frac{t_b{}^2 V_{DS}}{L^2}) \quad . \tag{4.31}$$

Notice that the limiting current expressions in (4.29) and (4.30) have a V_{DS}-dependent term, which has not been considered in [She87]. This dependence is needed to ensure that I_{WK} is always smaller than I_{ST} above threshold. Indeed when a MOSFET is on (strong inversion) and V_{DS} is small, I_{WK} is limited by I_{LIMIT}, which can be much larger than I_{ST} if the V_{DS}-dependent term is not included. The term we adopted is of

the same form as the V_{DS} terms in the $I_{cf(weak)}$ and $I_{cb(weak)}$ expressions, but could have different V_{DS} dependences as long as $I_{WK} < I_{ST}$ is guaranteed for all V_{DS}.

Note in (4.29) and (4.30) that the limiting current is given by a strong-inversion saturation current expression with the gate voltage just a few (n) times V_{th} above the threshold voltage. This is physically based; as the gate voltage increases and surpasses the threshold voltage, the device is actually in the saturation region in most cases. Hence the limiting current chosen can be regarded as a proper one. We also note that n should be chosen to ensure that the channel current at $V_{GfS} = V_{Tf}$ is approximately equal to the weak-inversion current rather than the strong-inversion current since the condition $\psi_{sf0} = 2\phi_B$ assumed in the V_{Tf} calculation is closer to weak inversion [Tsi82].

4.3 Parasitic BJT Model

In Chapter 3, the importance of parasitic BJT effects in fully depleted submicron SOI MOSFET was discussed. The main effects on DC device characteristics are the premature breakdown and the off-state latch. In this section, the recombination current and the base transport current of the BJT are derived based on the physical insight gained through the PISCES simulations in Chapter 3. The recombination current model, which dictates the significance of the BJT,

accounts for the effects of an LDS region, and includes doping-dependent carrier mobility and lifetime.

4.3.1 Recombination Current at Source-Body Junction

From PISCES simulations in Chapter 3, we find that the dominant recombination occurs at the quasi-neutral source region. Recombination in the fully depleted film body, including the metallurgical junction region, is small due to carrier separation by the vertical field and because the carrier lifetime in the body is longer than that in the higher-doped source. This situation is reflected by the PISCES-predicted body-source bias (V_{BS}) dependence of the recombination current: $I_R \propto \exp(V_{BS}/V_{th})$ even for very low V_{BS} as shown in Fig. 3.5. Based on this observation, we model the recombination current by analyzing the minority-hole transport in the quasi-neutral source, which may include an LDS region.

Figure 4.3 is a one-dimensional illustration of the source structure including an LDS. As shown, N_{DS} and N_{LDS} are the n^+ source and LDS doping densities, respectively, which are assumed uniform. The n^+ source length is L_S, which is the effective space between the source contact and n^+-n^- junction in an actual (three-dimensional) device. The LDS length is L_{LDS}. The important recombination current is

$$I_R = W\, t_b\, J_p(0) \qquad (4.32)$$

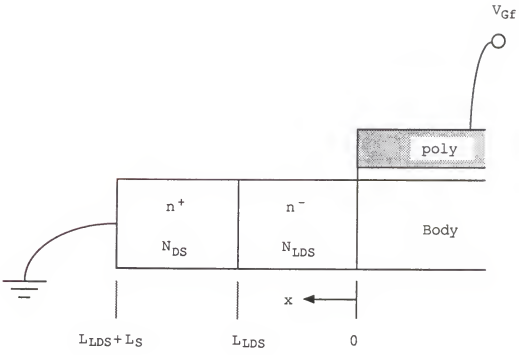


Fig. 4.3 A one-dimensional representation of the source structure including an LDS.

where $J_p(0)$ is the injected hole current density. Assuming one-dimensional current flow, we write the hole continuity equation for steady state as

$$\frac{1}{q}\frac{dJ_p(x)}{dx} + \frac{\Delta p(x)}{\tau_p} = 0 \tag{4.33}$$

with

$$J_p(x) = - q\, D_p \frac{dp(x)}{dx} + q\, \mu_p\, E_p\, p(x) \tag{4.34}$$

where τ_p, μ_p, and D_p ($= V_{th}\, \mu_p$) are lifetime, mobility, and diffusivity for the holes, respectively. We note that the excess hole density $\Delta p \equiv p$ since the equilibrium hole density is negligible, and hence p and Δp will be used interchangeably.

In (4.34), E_p is the (effective) electric field influencing the holes. This field can be developed in the LDS region due to an ohmic drop caused by majority-electron current. In this case, we assume

$$E_p = \frac{I}{q\, W\, t_b\, N_{LDS}\, \mu_{n(LDS)}} \tag{4.35}$$

where $\mu_{n(LDS)}$ is the electron mobility in the LDS region and I is the total electron current flowing this region. In the LDS then, (4.33) and (4.34) yield

$$\frac{d^2\Delta p}{dx^2} - \frac{E_p}{V_{th}} \frac{d\Delta p}{dx} - \frac{\Delta p}{\mu_{p(LDS)} V_{th} \tau_{p(LDS)}} = 0 \qquad (4.36)$$

where $\mu_{p(LDS)}$ and $\tau_{p(LDS)}$ are the hole mobility and lifetime in the region. The general solution of (4.36) is

$$\Delta p(x) = A_1 \exp(m_1 x) + B_1 \exp(m_2 x) \qquad (4.37)$$

where

$$m_1, m_2 = \frac{\frac{E_p}{V_{th}} \pm \left[\left(\frac{E_p}{V_{th}}\right)^2 + \frac{4}{\mu_{p(LDS)} V_{th} \tau_{p(LDS)}}\right]^{1/2}}{2} \qquad (4.38)$$

In the heavily doped n^+ region, we assume $E_p = 0$ for the uniform-doping case. In fact, even for nonuniform doping, we can assume $E_p \cong 0$ since a quasi-field due to bandgap narrowing tends to nullify the built-in field due to the doping gradient [Fos82]. Hence (4.33) and (4.34) with $E_p = 0$ yield

$$\frac{d^2\Delta p}{dx^2} - \frac{\Delta p}{\mu_{p(S)} V_{th} \tau_{p(S)}} = 0 \qquad (4.39)$$

where $\mu_{p(S)}$ and $\tau_{p(S)}$ are the hole mobility and lifetime in n^+ region. The general solution of (4.39) is

$$\Delta p(x) = A_2 \exp\left(\frac{x - L_{LDS}}{\sqrt{\mu_{p(S)} V_{th} \tau_{p(S)}}}\right) + B_2 \exp\left(-\frac{x - L_{LDS}}{\sqrt{\mu_{p(S)} V_{th} \tau_{p(S)}}}\right) \qquad (4.40)$$

(4.37) and (4.40) are the two regional solutions for the excess hole density in the source, which will define I_R. The solutions must be coupled by evaluating the coefficients with the following boundary conditions:

$$\Delta p(L_{LDS}+L_S) = 0 \quad , \tag{4.41}$$

$$\Delta p(L_{LDS}{}^{+}) = \frac{n_i{}^2}{N_{D(eff)}} \left[\exp\left(\frac{V_{BS}{}'}{V_{th}}\right) - 1\right] \quad , \tag{4.42}$$

$$\Delta p(L_{LDS}{}^{-}) = \frac{n_i{}^2}{N_{LDS}} \left[\exp\left(\frac{V_{BS}{}'}{V_{th}}\right) - 1\right] \quad , \tag{4.43}$$

$$\Delta p(0) = \frac{n_i{}^2}{N_{LDS}} \left[\exp\left(\frac{V_{BS}}{V_{th}}\right) - 1\right] \quad , \tag{4.44}$$

and

$$J_p(L_{LDS}{}^{+}) = J_p(L_{LDS}{}^{-}) \quad , \tag{4.45}$$

where V_{BS} is the quasi-Fermi potential separation at the source-body junction (x = 0), and $V_{BS}{}'$ is the quasi-Fermi potential separation at the n^+-n^- junction (x = L_{LDS}). $N_{D(eff)}$ is the effective n^+ source doping density, which is less than N_{DS}, and approximately equal to a constant value of about 10^{18} cm^{-3} for $N_{DS} > 10^{18}$ cm^{-3} due to the heavy-doping effects [Fossu81]. Notice that there are five unknowns (A_1, B_1, A_2, B_2, and $V_{BS}{}'$) with five boundary conditions in the model. After solving this system of equations in terms of V_{BS}, we evaluate $J_p(0)$ by (4.34), and write I_R in (4.32) as

$$I_R = \frac{qWt_b n_i^2}{N_{LDS}} \mu_{p(LDS)} \left[E_p - \frac{V_{th}(m_1+m_2C)}{1+C}\right]\left[\exp\left(\frac{V_{BS}}{V_{th}}\right) - 1\right] \qquad (4.46)$$

where

$$C = \frac{\mu_{p(LDS)}E_p - \mu_{p(LDS)}V_{th}m_1 - K}{-\mu_{p(LDS)}E_p + \mu_{p(LDS)}V_{th}m_2 + K} \exp\left[(m_1-m_2)L_{LDS}\right] \qquad (4.47)$$

with

$$K = \frac{N_{LDS}}{N_{D(eff)}} \left(\frac{\mu_{p(S)}V_{th}}{\tau_{p(S)}}\right)^{1/2} \frac{\exp\left(\frac{2L_S}{\sqrt{\mu_{p(S)}V_{th}\tau_{p(S)}}}\right) + 1}{\exp\left(\frac{2L_S}{\sqrt{\mu_{p(S)}V_{th}\tau_{p(S)}}}\right) - 1} \quad . \qquad (4.48)$$

For the limiting case where there is no LDS, with $L_{LDS} = 0$, (4.46) reduces to a simpler form:

$$I_R = \frac{qWt_b n_i^2}{N_{LDS}} K \left[\exp\left(\frac{V_{BS}}{V_{th}}\right) - 1\right] \quad . \qquad (4.49)$$

4.3.2 Base Transport Current

As discussed in Chapter 3, high-level injection is common in the fully depleted, floating body of the short-channel SOI MOSFET. Upon injection of holes, for example, by impact-ionization generation near drain, an injection of electrons from the source region is induced, and the electron and hole quasi-Fermi levels near the source junction shift simultaneously as in intrinsic material under injection. Even when the injected electron density is less than N_A, n and p

are about equal at the source-body junction, as for high-injection conditions. Since the film doping is usually low to ensure full depletion of the film body though, the actual condition of high injection generally prevails. Based on this observation, the base transport current associated with the BJT action is modeled by assuming high injection in the fully depleted body region.

The BJT transport current is approximately [Sze81]

$$I_T \equiv \frac{qWt_b n_i^2 \bar{D}_{n(B)}}{\int_{body} p \, dx} \left[\exp\left(\frac{V_{BS}}{V_{th}}\right) - 1\right] \tag{4.50}$$

where $\bar{D}_{n(B)}$ ($= \bar{\mu}_{nf} V_{th}$) is the average electron diffusivity in the body. Here $\bar{\mu}_{nf}$ is assumed to be given by (4.5) in the channel analysis, which is a good approximation since the injected electrons experience the same vertical field as the channel electrons. Assuming a linear distribution of holes in the highly injected film body, which is consistent with our implicit assumption of negligible recombination in the body [Sze81] that underlies (4.50), we write

$$\int_{body} p \, dx \equiv \frac{L_{ef}}{2} n_i \exp\left(\frac{V_{BS}}{2V_{th}}\right) + N_A L_{ef} \tag{4.51}$$

where the effective front-channel length L_{ef} is used as the effective base width. This approximation is justified by the fact that the carrier velocity is saturated in the drain

high-field region, and the transport of injected electrons is governed by (4.50) only within L_{ef}.

The combination of (4.50) and (4.51) model $I_T(V_{BS})$. Since L_{ef} is a function of V_{DS}, the BJT model basically includes the Early effect [Ear52]. Note that our assumption that the film is fully depleted may not be strictly valid in the off-state of the MOSFET. Since the BJT current gain β (= I_T/I_R) is proportional to $\exp(-V_{BS}/2V_{th})$ in high injection [Web54], the full-depletion approximation can result in unrealistically high β in the off-state when V_{BS} is small. To limit β in this case, a compromise is done by adding the N_A term in (4.51), which is significant only for low V_{BS}.

4.4 Effects of LDS and LDD

In short-channel MOSFETs, an LDD is typically used to control overall short-channel effects associated with the high drain field. An identical LDS is usually included to simplify the technology. Our analyses in Chapter 3 revealed that the LDS and LDD have unique roles in controlling the drain field and parasitic BJT effects. Modeling the LDS and LDD effects is complicated, and in fact is usually not done for circuit simulation. We must do it here, but some simplifications are made to keep the model practical. We assume uniform LDD and LDS doping, equal to N_{LDS} in both regions. We also assume no overlap of the gate oxide on the LDD or LDS region. These simplifications greatly reduce the

complexity of the model, which nonetheless is still capable of representative simulations.

4.4.1 Effects of LDS

Three major effects of the LDS are i) to reduce the parasitic BJT effect by increasing the source recombination current, as we explained in Chapter 3 and modeled in the previous section; ii) to reduce the body charge-sharing effect, thereby limiting the threshold voltage reduction in short-channel MOSFETs (and reducing the back-channel leakage by DIBL.); and iii) to increase the source resistance, thereby effectively reducing gate drive. The voltage drop across the LDS region can also affect the drain field by modifying the saturation characteristics. Models for the effects ii) and iii) are derived in this section.

4.4.1.1 Effect on Charge Sharing

The threshold voltage, defined for low V_{DS}, is reduced in short-channel MOSFETs because some portion of the depletion charge under the gate is controlled by the source and drain [Vis85]. The amount of charge shared is a function of the source and drain doping as well as the body doping. With an LDD and/or LDS, the magnitude of the shared charge is reduced. We note that the LDD has the same effect on charge sharing as the LDS, and the following model accounts for both the LDS and LDD regions.

The built-in source/drain junction potential is a function of the LDS/LDD doping, N_{LDS}, and it determines the magnitude of body charge shared by the source and drain. Built-in potential at each junction with an LDS/LDD is expressed by

$$V_{bi}(S,D) = V_{th} \ln\left(\frac{N_{LDS} N_A}{n_i^2}\right) \quad . \tag{4.52}$$

If there is no LDD or LDS, $V_{bi} \cong E_g/2 + V_{th} \ln(N_A/n_i)$ since the source/drain doping is high. The charge sharing is dictated by the effective lateral component of the electric field, $E_{b(eff)}$, at the back interface, defined by Eq. (3) in [Vee88b] for an asymmetric junction. Generalizing the model to include an LDS or LDD, we modify Eq. (3) to

$$E_{b(eff)}(S,D) = f_0 \left[\frac{qN_A(V_{bi}(S,D) - \psi^*_{sb0})}{2\,\varepsilon_s} \frac{N_{LDS}}{N_A + N_{LDS}}\right]^{1/2}$$

$$+ f_\alpha \frac{\varepsilon_{ox}}{\varepsilon_s} \frac{V_{GbS} - V_{FB}{}^b - \psi^*_{sb0}}{t_{ob}}$$

$$+ f_\beta \frac{\varepsilon_{ox}}{\varepsilon_s} \frac{-V_{GbS} + V_{FB}{}^b + \frac{V_{bi}(S,D) N_{LDS} + \psi^*_{sb0} N_A}{N_A + N_{LDS}}}{t_{ob}} \tag{4.53}$$

where ψ^*_{sb0} is the back-surface band bending for $V_{DS} = 0$ as defined in (4.13). Then the back-surface field penetration

into the body region from the source/drain junction is expressed as

$$d_{(S,D)} = \frac{V_{bi}(S,D) - \Psi^{*}_{sb0}}{E_{b(eff)}(S,D)} \frac{N_{LDS}}{N_A + N_{LDS}} \quad . \tag{4.54}$$

Approximating the component of body charge coupled to the gates as being confined to a trapezoidal region (see Fig. 2 of [Vee88b]), we write

$$Q_{b(eff)} = - q N_A t_b \left(1 - \frac{d_S + d_D}{2L}\right) \quad , \tag{4.55}$$

which is the effective body depletion charge used in the channel model (Section 4.2). If there is no LDS or LDD, (4.54) is reduced to Eq. (4) in [Vee88b].

4.4.1.2 Source Resistance

The voltage drop in the LDS region can be modeled by a simple bias-independent resistor. Assuming uniform current density across the LDS thickness, we express the drop simply as

$$V_{LDS} = I R_{LDS}$$

$$= I \frac{L_{LDS}}{q W t_b \mu_{n(LDS)} N_{LDS}} \tag{4.56}$$

where I is the total electron current. This model is consistent with the characterization of E_p in (4.35), which is part of the accounting for the LDS effect on the parasitic BJT.

4.4.2 Effects of LDD

Two major effects of the LDD are i) to reduce the charge-sharing effect, which was modeled in Section 4.4.1.1, and ii) to reduce the effective drain voltage due to the voltage drop V_{LDD} across the LDD region. This voltage drop, which results in a lower drain field, is a simple ohmic drop below saturation, but it is more complex above saturation. We note that the channel analysis in the previously developed model [Vee88b] is applicable with the effective drain voltage (V_{DS}-V_{LDD}) replacing V_{DS}. In this section, V_{LDD} is characterized. In the next section, it is used for the calculation of the reduced impact-ionization multiplication.

Similarly to the analysis of LDS region, we assume that the current density in the LDD region is uniform. We also assume that field modulation by injected carriers (electrons) is negligible in the LDD region, which is true for most practical LDD doping levels. Figure 4.4 shows a one-dimensional representation of the drain structure including an LDD, and drain-field distributions as a function of drain bias. The constant-field regions reflect neutrality and define simple ohmic drops. The graded-field regions reflect

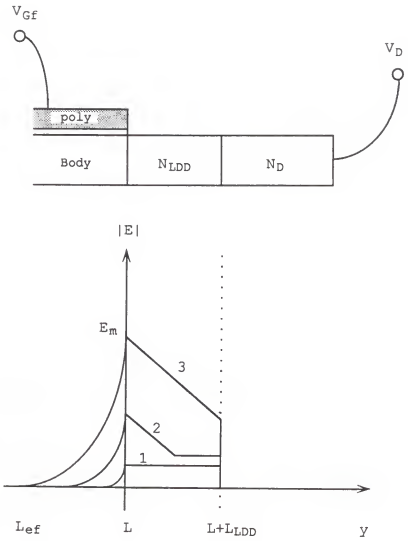


Fig. 4.4 A one-dimensional representation of the drain structure including an LDD, and possible cases of drain-field distribution as a function of V_{DS}.

depletion, which is induced in the LDD with a high channel field E_m. In the depletion region, Poisson's equation gives

$$\frac{d|E|}{dy} = \frac{-qN_{LDD}}{\varepsilon_s} \equiv -S \tag{4.57}$$

if the electron charge is negligible, showing a constant slope S for the field distribution.

The LDD analysis is linked to the channel analysis [Vee88a] by the maximum drain field under the gate

$$E_m = \frac{V_{DS} - V_{LDD} - V_{DS(eff)}}{l_c} \tag{4.58}$$

at the body-LDD junction. In (4.58), $V_{DS(eff)}$ is defined by Eq. (2.26) in [Vee88a] with V_{DS} replaced by $(V_{DS}-V_{LDD})$; L_{ef} in Eq. (2.26) is given by Eq. (26) in [Vee88b], again with V_{DS} replaced by $(V_{DS}-V_{LDD})$.

The internal saturation voltage $V_{DS(sat)}^*$, which is the voltage across the channel from the source-body junction to the drain-body junction at the onset of saturation, defines the mode of transport in the LDD. $V_{DS(sat)}^*$ is defined by Eq. (2.26) in [Vee88a] with $L_{ef} = L$. For $(V_{DS}-V_{LDD}) \leq V_{DS(sat)}^*$, we assume E_m is small such that only the ohmic drop at the LDD region is important. Hence the field distribution '1' in Fig. 4.4 is used to calculate V_{LDD} in this case. For $(V_{DS}-V_{LDD}) > V_{DS(sat)}^*$, all three cases '1', '2', and '3' are possible. If E_m is less than the constant field $(=Ir_D)$, the field

distribution '1' is used. As V_{DS} increases, the space-charge region expands to give the field distribution '2'. If the entire LDD region is space-charged with higher V_{DS}, '3' is applied. The transition from '2' to '3' is defined by the condition $(E_m - Ir_D) = SL_{LDD}$, as can be seen in Fig. 4.4 with (4.57). Here I is the current flowing through LDD region, and r_D is the LDD resistance per unit LDD length, which is defined as

$$r_D = \frac{1}{q\ W\ t_b\ N_{LDD}\ \mu_{n(LDD)}} \tag{4.59}$$

where $\mu_{n(LDD)}$ is the electron mobility in this region.

Quantitatively then, for $(V_{DS}-V_{LDD}) \leq V_{DS(sat)}^*$, the field distribution '1' gives

$$V_{LDD} = I\ r_D\ L_{LDD} \quad . \tag{4.60}$$

Even though $(V_{DS}-V_{LDD}) > V_{DS(sat)}^*$, (4.60) is still applied if $E_m \leq Ir_D$. However for $E_m > Ir_D$, the LDD region cannot be modeled as a simple resistor anymore due to the voltage drop in the space-charge region. If $(E_m - Ir_D) \leq SL_{LDD}$, the field distribution '2' is applicable, and

$$V_{LDD} = \frac{(E_m - Ir_D)^2}{2S} + Ir_D L_{LDD} \quad . \tag{4.61}$$

If $(E_m - Ir_D) > SL_{LDD}$, '3' is applicable, and

$$V_{LDD} = 0.5\ L_{LDD}(2E_m - SL_{LDD}) \quad . \tag{4.62}$$

The above model is applicable for both strong and weak inversion. In weak inversion, $V_{DS(sat)}{}^*$ and $V_{DS(eff)}$ are equal to only a few times V_{th}, and are approximated by zero in calculating E_m in (4.58). Notice here that V_{LDD}, $V_{DS(eff)}$, E_m, and I are strongly coupled to each other, which indicates an inevitable iterative solution procedure, discussed in Chapter 5. Continuity of V_{LDD} and E_m is guaranteed in the model.

4.4.3 Impact Ionization in the LDD Region

With an LDD included, impact ionization can occur in the LDD as well as under the gate (as modeled previously). The carrier multiplication in the channel region, $(M-1)_{CH}$, is described by Eq. (31) in [Vee88b], but with the modified E_m in (4.58). As in the previous model, we neglect the multiplication below saturation (Case '1'). For Case '2', we neglect the multiplication in the neutral LDD region where E is relatively low, since (M-1) is an exponential function of E. Therefore we write the multiplication inside the LDD for Cases '2' and '3' assuming weak impact ionization as

$$(M-1)_{LDD} = \int_{L}^{L+L_{LDD}} \alpha_0 \exp\left(-\frac{\beta_0}{|E|}\right)\, dy$$

$$\cong \int_{E_m}^{E_m-SL_{LDD}} \alpha_0 \exp(-\frac{\beta_0}{|E|}) \frac{dy}{d|E|} d|E|$$

$$= \frac{\alpha_0}{S} \int_{E_m-SL_{LDD}}^{E_m} \exp(-\frac{\beta_0}{|E|}) d|E| \qquad (4.63)$$

where α_0 and β_0 are the impact-ionization constants. In (4.63) the lower limit for integration is (E_m-SL_{LDD}) or 0 whichever is larger. This integral cannot be transformed into a simple analytical form, but can be easily evaluated by numerical integration. The total multiplication, (M-1), is the sum of $(M-1)_{CH}$ and $(M-1)_{LDD}$, and the impact-ionization current is defined by

$$I_{Gi} = (M-1)(I_{CH} + I_T) \quad . \qquad (4.64)$$

Here the thermal generation current is assumed not multiplied by impact ionization. Since a significant part of thermal generation occurs in the high-field region where impact ionization occurs, it is not likely for the thermally generated electrons to gain enough kinetic energy for impact ionization for conditions commensurate with only weak impact ionization as assumed in the model.

4.5 Thermal Generation Current

Since the BJT-related latch can be triggered by the thermal generation leakage current I_{Gt}, we include a carrier

lifetime-dependent I_{Gt} model. However, to keep the model as simple as possible, we assume generation occurs in the whole body region, which is assumed fully depleted for all bias conditions. With this approximation, I_{Gt} is expressed as

$$I_{Gt} = q \int_{Body} |U| \, dV$$

$$\cong \frac{q \, n_i \, W \, t_b \, L}{\tau_G} \tag{4.65}$$

where U is the generation rate, and τ_G is the generation lifetime inside the film body, which is about equal to the sum of electron and hole lifetimes [War83].

4.6 Mobility and Lifetime Model

To provide proper evaluation of mobilities and lifetimes in the model equations of Sections 4.3-4.5, doping dependences are introduced in this section. These dependences include an empirical characterization for $\mu_{n(LDS)}$, $\mu_{n(LDD)}$, $\mu_{p(LDS)}$, $\mu_{p(S)}$, and a semi-empirical model for $\tau_{p(LDS)}$, $\tau_{p(S)}$, and τ_G.

4.6.1 Doping-Dependent Mobility Model

The empirical mobility characterization in [Mul77] is used in the model:

$$\mu = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + (\frac{N}{N_{ref}})^{\alpha}} \tag{4.66}$$

where μ is the desired doping-dependent mobility, and N is the doping density in the region where mobilities are calculated. N_{ref} and α are empirical constants, and μ_{max} and μ_{min} are the maximum and minimum mobility values respectively. For n-type silicon, we use $N_{ref} = 1.3 \times 10^{17}$ cm^{-3}, $\alpha = 0.91$, $\mu_{max} = 1360$ $cm^2/V\text{-sec}$, and $\mu_{min} = 92$ $cm^2/V\text{-sec}$. For p-type silicon, we use 6.3×10^{16} cm^{-3}, 0.76, 495 $cm^2/V\text{-sec}$, and 47.7 $cm^2/V\text{-sec}$, for the respective values.

4.6.2 Doping-Dependent Carrier Lifetime Model

Carrier lifetime is constant for lower doping density, and decreases inversely with increasing doping density above about 10^{17} cm^{-3} due to Shockley-Read-Hall (SRH) recombination and the inherent nearly linear dependence of trap density on doping density. However, for higher doping, the lifetime decreases faster showing a quadratic dependence due to the band-band Auger process [Foss83]. Therefore the lifetime must be defined by two parallel recombination mechanisms:

$$\frac{1}{\tau} = \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{BBA}} \tag{4.67}$$

where τ is the doping-dependent carrier lifetime, τ_{SRH} is the carrier lifetime defined by the SRH process, and τ_{BBA} is the

carrier lifetime defined by the Auger process. Following [Rou82], τ_{SRH} is given as

$$\tau_{SRH} = \frac{\tau_0}{1 + N/N_{SRH}} \tag{4.68}$$

where N_{SRH} is an empirical constant of $5x10^{16}$ cm^{-3}, τ_0 is the lifetime at low doping well below N_{SRH}, and N (cm^{-3}) is the doping density in the region of interest. τ_{BBA} is given by

$$\tau_{BBA} = \frac{1}{C\ N^2} \tag{4.69}$$

where N is the doping density in cm^{-3} and C is the Auger coefficient, which is 10^{-31} cm^6/sec for p^+ material and about $2x10^{-31}$ cm^6/sec for n^+ material [Foss83].

4.7 Charge Dynamics

The previously developed model [Vee88b] for charge dynamics is applied with the internal source-to-drain and the internal source-to-gate voltages (affected by V_{LDD} and V_{LDS}) replacing the terminal voltages V_{DS} and V_{Gfs}. The possible changes in charge dynamics are related to the subthreshold weak-inversion charges and the charges related to parasitic BJT. Since weak-inversion charge is negligible compared with the body depletion charge Q_b, no modification is considered relating subthreshold conduction. Also the charge related to parasitic BJT is not modeled in this work. This

simplification is justified by the fact that design should eliminate the BJT-related problems in DC device characteristics, which will ensure that the charge dynamics related to BJT action is insignificant in transient situations.

4.8 Summary

Models for subthreshold conduction, effects of LDS and LDD, parasitic BJT effects, and thermal generation current were derived based on the analyses in Chapter 3. Semi-empirical mobility and carrier lifetime models were introduced to complete the model. The resulting model for the fully depleted SOI MOSFET structure is a useful tradeoff between accuracy and complexity, based on several key simplifying approximations. A good linkage to the previously developed model [Vee88b] was ensured in the model derivation. The model for parasitic BJT effects was aimed to provide a capability to simulate especially the DC device characteristics, keeping the complexity of the overall charge model reasonable for transient device/circuit simulations.

CHAPTER 5
MODEL IMPLEMENTATION IN SOISPICE-2

5.1 Introduction

The network representation of the comprehensive SOI MOSFET model developed in Chapter 4 is shown in Fig. 5.1. In this chapter, we define the model algorithm, that is the sequence of analyses needed to evaluate all currents and charges corresponding to a specified set of terminal voltages. We also describe the implementation of the model routine into the source code of the circuit simulator SPICE2 [Nag75] to create "SOISPICE-2".

The previously developed SOISPICE [Fit89] is an enhanced version of SPICE2 which includes the short-channel SOI MOSFET model described in [Vee88b]. This model allows two modes of device operation (TFA and TFD) as discussed in Chapter 2. However SOISPICE-2, while equipped with the more comprehensive model, allows only the TFD mode of operation. This mode is in fact the most advantageous and practical with regard to rendering the fully depleted SOI CMOS technology truly competitive with bulk CMOS in commercial digital VLSI applications. We note, in contrast to the previous four-terminal TFD model [Vee88b], that the new model is five-

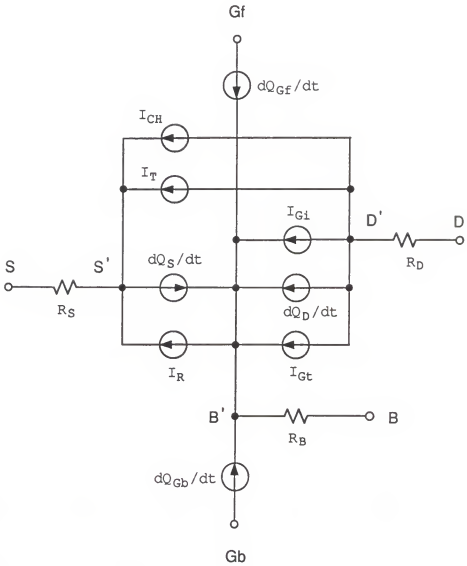


Fig. 5.1 Network representation of the quasi-static large signal model for the fully depleted SOI MOSFET.

terminal, including the front gate, the back gate, the source, the drain, and the body, which can be biased, for example, to monitor the impact ionization current I_{Gi}.

Because of the major extensions of the model, described in Chapter 4, the algorithm is completely new, including the addition of two main iteration loops associated with the LDS and LDD. We therefore give a detailed description of the implementation to facilitate future source-code modifications for model refinement. Section 5.2 is devoted to this purpose. The overall structure of SOISPICE-2 is described in Section 5.2.1. The algorithm for the model routine SOIMOD is discussed in Section 5.2.2, with the description of the model parameters. The subthreshold model subroutine is discussed in Section 5.2.3. In Section 5.2.4, the numerical techniques now needed for solving the model equations are described. They were chosen to optimize the computational efficiency and to maximize convergence. The simplifications and consequent limitations of the model are indicated throughout Section 5.2.

In Section 5.3, SOISPICE-2 device and circuit simulation results showing the effects of the new features in the model are presented to demonstrate the capability of the simulator. Computation times corresponding to various combinations of the new model features are given to indicate computational efficiency. An example is also presented to show the capability and efficiency of SOISPICE-2 in simulating a

rather large circuit. The collection of the simulations presented serves to demonstrate how the tool functions as a "semi-numerical mixed-mode device/circuit simulator".

In developing SOISPICE-2, a stand-alone model routine, equivalent to SOIMOD, was written for test purposes prior to linking SOIMOD to SPICE2. The source code for this separate routine, written in FORTRAN, is given in Appendix. Note that it, different from SOIMOD, includes an additional loop to calculate the floating-body potential. (In SOISPICE-2, this calculation is part of the circuit nodal analysis.) This program, which is restricted to DC simulations, is useful for debugging and further enhancement of the model since any variable in the model can be easily printed out, and effects of modifications can be quickly checked. Such capability is constrained in SOISPICE-2.

5.2 Software Development

5.2.1 Overall Structure of SOISPICE-2

In SOISPICE-2, the SOI MOSFET model is accessed similarly to other semiconductor device models written into SPICE2. The source-code modification of the circuit simulator comprises four new device routines, SOIFET, SOIID, SOIEC, and SOIMOD, and changes in 16 of the original routines in SPICE2 to accept the new model. The four separate device routines are used for the SOI MOSFET model to facilitate handling the implicit nature of the model.

SOIFET is the first-level device routine for DC and transient simulation of SOI MOSFETs. SOIFET initializes variables used in the internal iterations of the model routine based on previous values of the variables and on their dependences on the terminal voltage differences, V_{DS}, V_{GfS}, V_{GbS}, and V_{BS}. This routine also links the model to the SPICE2 nodal analysis by doing other initializations, iterate limiting, and admittance-matrix (Y and RHS) load operations. The extrinsic resistances R_S, R_D, and R_B in Fig. 5.1 are treated as conductance elements in SOIFET; that is, their reciprocal values are directly added into the Y matrix.

SOIFET calls SOIID, which calculates the operating-point currents and charges by calling the model routine SOIMOD. SOIID also calculates the partial (voltage-) derivatives such as conductances and capacitances. Since analytical derivatives do not exist for the currents and charges in the semi-numerical model, numerical (divided-difference) approximations for the derivatives are used in the Newton-Raphson iterations of SPICE2. The numerical derivatives are calculated in SOIID via successive calls of SOIMOD with perturbed values of V_{DS}, V_{GfS}, V_{GbS}, and V_{BS}.

During transient analysis, SOIFET also calls SOIEC, which calculates equivalent conductances of the transcapacitances calculated in SOIID, based on the Backward-Euler integration method. We note that this method is fixed independently of the integration methods chosen for the nodal

analysis. SOIEC also calculates charges and equivalent conductances due to the extrinsic overlap capacitances. The equivalent conductances are added into the Y matrix in SOIFET, and are used to calculate the equivalent current sources which are added into the RHS matrix.

The model developed in Chapter 4 was written into SOIMOD through the algorithm described in the next section. Intermediate parameters, which are used as constants in SOIMOD throughout the simulation, are calculated in MODCHK using model (input) parameters, prior to the iterative nodal (and model) analysis.

It is not shown in Fig. 5.1, but the effective internal voltages used for current and charge calculations differ from the voltages between nodes S', D', B', Gb, and Gf due to the voltage drops in the LDS and LDD regions. Regarding its voltage drop, the LDS is treated as a simple resistor whose value is calculated from the structural parameters in MODCHK. This resistor could have been treated more simply in SOIFET together with R_S. However the iteration loop for the voltage drop in the LDS region is included in SOIMOD because the conductance matrix for the equivalent circuit needs to be symmetrical to allow for inverse-mode operation (with source and drain reversed). The symmetry is required, for example, when the bias on an n-channel MOSFET is switched to make the drain voltage lower than the source voltage. This situation typically occurs in the operation of transfer gates in CMOS

ICs. If there is no LDS and LDD, the source and the drain voltages are simply interchanged in the inverse mode. However if there is an LDS, the LDS resistor cannot be relocated within the conductance matrix, hence necessitating an inclusion in SOIMOD, which requires the additional, intensive (outer-) iteration loop.

5.2.2 Detailed Model Algorithm

Table 5.1 lists the new SOI MOSFET model parameters in SOISPICE-2. Definitions and their default values are given. As shown in the list, ETA and LMOD are the multipliers to turn on and off the DICE and channel-length modulation models [Vee88b] respectively. A zero value turns off the associated model. The models for charge sharing (ZETA), impact ionization (ALPHA and BETA), LDS (LDS), and LDD (LDD) can also be turned off by setting the noted parameter values to zero. The parasitic BJT model is turned on by stating 'BJT' in the device card. The fitting parameter for the subthreshold current, LIMFAC, can be used to turn off the weak-inversion model by setting its value to zero.

In Fig. 5.2, the overall algorithm of SOIMOD is flowcharted. For each Newton-Raphson iteration in the circuit nodal analysis, the internal node voltage differences, $V_{GfS'}$, $V_{D'S'}$, $V_{GbS'}$, and $V_{B'S'}$ in Fig. 5.1, but hereinafter called V_{GfS}, V_{DS}, V_{GbS}, and V_{BS} for simplicity, are passed into

TABLE 5.1
SOISPICE-2 SOI MOSFET MODEL PARAMETERS

Name	Description	Units	Default
(Intrinsic)			
VFBF	Front-gate flatband voltage	V	calc.
VFBB	Back-gate flatband voltage	V	calc.
WKF	Front-gate work function difference	V	calc.
WKB	Back-gate work function difference	V	calc.
NQFF	Fixed charge, front gate-oxide	$1/cm^2$	0.0
NQFB	Fixed charge, back gate-oxide	$1/cm^2$	0.0
TOXF	Front gate-oxide thickness	m	2.0e-8
TOXB	Back gate-oxide thickness	m	0.5e-6
NSUB	Substrate doping density	$1/cm^3$	1.0e14
NGATE	Polisilicon gate doping density	$1/cm^3$	1.0e19
TPG	Type of gate material +1) opposite to body -1) same as body 0) aluminum	-	0
TPS	Type of substrate +1) opposite to body -1) same as body	-	1
TB	Film (body) thickness	m	0.1e-6
PHIB	Twice Fermi potential of body	V	calc.
NBODY	Film (body) doping density	cm	5.0e15
U0	Zero field mobility	cm^2/Vs	700
THETA	Mobility degradation coefficient	cm/V	0.0
BFACT	V_{DS}-averaging factor for μ-degradation	-	0.0
VSAT	Saturated carrier velocity	cm/s	1.0e7
ZETA	charge-sharing parameter f_0 (0 for no charge sharing)	-	1.0
QSMA	charge-sharing parameter f_α	-	0.0
QSMB	charge-sharing parameter f_β	-	0.0
ALPHA	Impact-ionization parameter α_0	1/cm	1.0e6
BETA	Impact-ionization parameter β_0 (0's for no impact ionization)	V/cm	2.0e6
LIMFAC	Subthreshold fitting parameter n	-	3.0
TAU0	Carrier lifetime in lightly doped region	s	1.0e-6

(contd..)

TABLE 5.1 -- continued

Name	Description	Units	Default
LDS	LDS region length (0 for no LDS model)	m	0.0
LDD	LDD region length (0 for no LDD model)	m	0.0
NLDS	LDS/LDD doping density	$1/cm^3$	3.0e17
NDS	Source/drain doping density	$1/cm^3$	5.0e19
LS	Effective length of highly doped source region	m	0.5e-6
ETA	On/off multiplier for DICE model	-	1.0 (on)
LMOD	On/off multiplier for channel-length modulation model	-	1.0 (on)
(Extrinsic)			
CGFDO	Gate-drain overlap capacitance	F/m	0.0
CGFSO	Gate-source overlap capacitance	F/m	0.0
CGFBO	Gate-body overlap capacitance	F/m	0.0
RHOSD	Source and drain sheet resistance	Ω/square	0.0
RHOB	Body sheet resistance	Ω/square	0.0
RD	Drain parasitic resistance	Ω	0.0
RS	Source parasitic resistance	Ω	0.0
RB	Body parasitic resistance	Ω	0.0
DL	Channel-length reduction	m	0.0
DW	Channel-width reduction	m	0.0

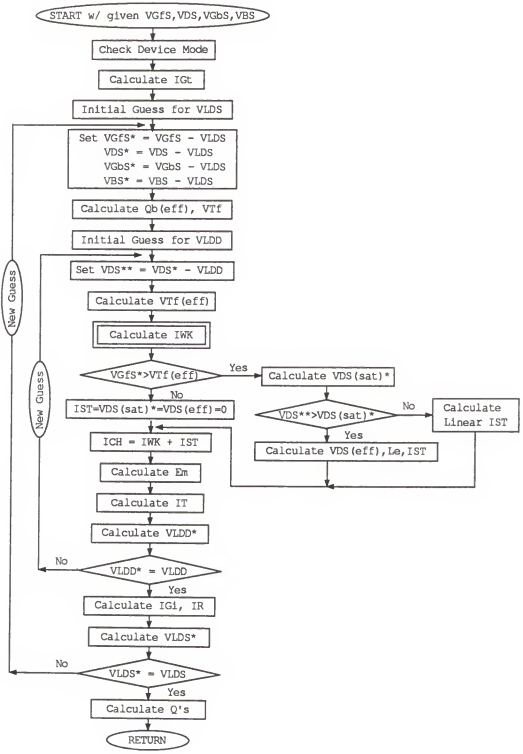


Fig. 5.2 Overall algorithm of the model routine SOIMOD.

SOIMOD, and all current components and charge components are calculated and returned to SOIID.

The first step in the algorithm is to determine whether the device is in the normal or inverse mode of operation. This determination is based on the sign of V_{DS} in SOIFET. If the device is in the inverse mode ($V_{DS} < 0$), the lengths of the LDS and LDD regions are interchanged in SOIMOD. If the device has only an LDS, it will behave like a device with only an LDD in the inverse mode.

The thermal generation current I_{Gt} is first calculated; it was modeled as a constant in Section 4.5. To force this current component to be zero at $V_{BD} = 0$, which is physically needed, and to be continuous as a function of V_{BD}, which is needed for convergence, we express I_{Gt} as

$$I_{Gt} = \frac{q\, n_i\, W\, t_b\, L}{\tau_G} \left[1 - \exp\left(\frac{V_{BD}}{V_{th}}\right)\right] \qquad (5.1)$$

where the term prior to the brackets was derived in Section 4.5. We note that (5.1) is similar to the current expression of a pn diode, but it has meaning only for $V_{BD} \leq 0$, which in fact will obtain for all common modes. The magnitude of V_{BD} represents the reverse bias on the body-drain junction, and it should be reduced by the voltage drop in the LDD region. However the effect of this voltage drop on I_{Gt} is neglected to reduce the complexity of the routine. This neglect is expected to cause only a minor change in the terminal-voltage

dependence of I_{Gt}, which generally is described by the coefficient in (5.1).

The next step is the initial guess for V_{LDS}, which is the voltage drop across the LDS region. For the first iteration, $V_{LDS} = 0$ is assumed. The internal terminal voltages V_{GfS}^*, V_{DS}^*, V_{GbS}^*, and V_{BS}^* are then defined as indicated in Fig. 5.2. Then Ψ_{sb0}^* and $Q_{b(eff)}$ are calculated by iteratively solving (4.53)-(4.55) and (4.13); and V_{Tf} is calculated by (4.12). The iteration method involved is discussed in Section 5.2.4.

The next step is the initial guess for V_{LDD}, which is the voltage drop across the LDD region. For the first (inner-loop) iteration, $V_{LDD} = 0$ is assumed. The effective drain-to-source voltage V_{DS}^{**} is then set equal to $(V_{DS}^* - V_{LDD})$. With V_{DS}^{**}, the effective threshold voltage $V_{Tf(eff)}$ is calculated based on (4.26). $V_{Tf(eff)}$ is calculated to define the onset (threshold) of strong inversion in the routine; it also facilitates the coding for strong-inversion current and charge expressions.

For all bias conditions, the weak-inversion current I_{WK}, as characterized in Section 4.2, is then calculated. The detailed algorithm for the I_{WK} calculation is described in Section 5.2.3. After I_{WK} is calculated, the strong-inversion model is evaluated. If the device is above threshold, the internal saturation voltage $V_{DS(sat)}^*$ is calculated by iteratively solving Eq. (2.26) in [Vee88a] and Eq. (21) in

[Vee88b] with $L_{ef} = L$. If V_{DS}^{**} is equal to or smaller than $V_{DS(sat)}^{*}$, the strong-inversion current I_{ST} in the linear (triode) region is evaluated using Eq. (20) in [Vee88b] with $L_{ef} = L$. If V_{DS}^{**} is larger than $V_{DS(sat)}^{*}$, $V_{DS(eff)}$, L_{ef}, and the effective mobilty are calculated by iteratively solving Eq. (2.26) in [Vee88a] and Eqs. (21) and (26) in [Vee88b], and the saturation region I_{ST} is evaluated using Eq. (20) in [Vee88b]. If the device is below threshold, $V_{DS(sat)}^{*}$, $V_{DS(eff)}$, and I_{ST} are set equal to zero. (The iteration method involved is discussed in Section 5.2.4.) Finally the total channel current is defined by $I_{CH} = I_{ST} + I_{WK}$.

The next step is the estimation of the maximum drain field E_m by (4.58). It is set equal to zero if the device is below saturation. The BJT base transport current I_T is then determined by (4.50) and (4.51), if the BJT flag is on.

A new V_{LDD} value (V_{LDD}^{*}) is then calculated using the LDD model described by (4.60)-(4.62). Here the total current used for the calculation of the possible ohmic drop in the LDD region is simplified as a sum of I_{CH} and I_T. The impact-ionization current I_{Gi} is not included since it is expected to be relatively small for typical conditions. Indeed the characterization of I_{Gi} in Chapter 4 is based on the assumption of weak impact ionization. I_{Gt} is also neglected since it is small for all biases. To simplify the problem, we neglect the transient charging current dQ_D/dt [Vee88b], which is mainly the current associated with the partitioned channel

charge. If necessary, dQ_D/dt may be approximated by the dQ_D/dt value at the previous time step to avoid the excessive and prohibitive complexity of the exact formalism. However even this simplification will hamper the convergence greatly.

The new V_{LDD} is compared with the old one. If they are not equal, subject to an error tolerance, a new guess by a hybrid secant-bisection method [Jeo89] is returned to the beginning of the LDD (inner) loop; we note that the second initial guess was chosen as 0.4 times V_{DS}^*. This iterate-control method increases the computational efficiency significantly and reduces convergence problems by bracketing the iterate within a certain interval. It will be discussed briefly in Section 5.2.4.1.

If the convergence criterion is met, I_{Gi} and I_R are evaluated. For I_{Gi} calculation, the impact-ionization multiplication factor in the channel region, $(M-1)_{CH}$, is first calculated based on Eq. (31) in [Vee88b]. As mentioned in Chapter 4, the multiplication factor in the LDD region, $(M-1)_{LDD}$, is calculated based on (4.63) by a numerical integration. Romberg's integration method [Chen85], which is an algorithm combining the trapezoidal method with Richardson extrapolation, was chosen to increase the computing efficiency. The sum of $(M-1)_{CH}$ and $(M-1)_{LDD}$ are used to calculate I_{Gi} by (4.64). I_R is evaluated by (4.49) for the no-LDS case, or by (4.46)-(4.48) for the LDS case.

In the next step, a new V_{LDS} value (V_{LDS}^*) is calculated by $V_{LDS} = I\ R_{LDS}$. Here I is the total electron current, which is taken as the sum of I_{CH} and I_T. The charging current dQ_S/dt [Vee88b] is neglected for simplicity analogous to the neglect of dQ_D/dt in the V_{LDD} calculation. If the new V_{LDS} value is not equal to the old one within an error tolerance, a new guess by the hybrid secant-bisection method is returned to the beginning of the LDS (outer) loop; the second initial guess was chosen as 0.1 times V_{DS}.

If the convergence criteria are met, the charge terms associated with all terminals are calculated in terms of the internal terminal voltages as outlined in Chapter 4. All current and charge components are then returned to the calling routine (SOIID).

5.2.3. Subthreshold-Current Calculation

Figure 5.3 illustrates the procedure of calculating the subthreshold current I_{WK} within the inner loop in Fig. 5.2. As mentioned in Chapter 4, I_{WK} is evaluated for all bias conditions, and even well above threshold to eliminate any discontinuity problem.

The first step is to evaluate the front-surface band bending ψ_{sf} by (4.19), which is valid only for weak inversion. Notice that the parenthesized term in (4.19) is equal to $(V_{GfS}-V_{Tf(eff)})$, which is calculated prior to I_{WK} calculation. As evident in (4.19), ψ_{sf} can be mathematically less than

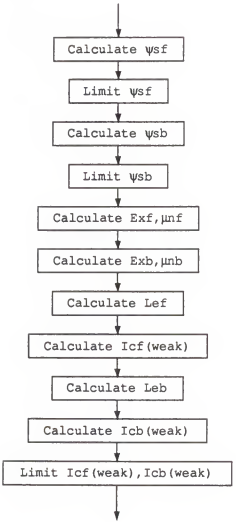


Fig. 5.3 Procedure of the I_{WK} calculation.

zero, which is not physical. Also it can be larger than $2\phi_B$, which is the assumed surface band bending at threshold. We note that both cases are inconsistent with our weak-inversion assumption underlying (4.19). However limiting the minimum and maximum value of ψ_{sf} in (4.8), the expression for $I_{cf(weak)}$, is not needed for the calculation. When $\psi_{sf} < 0$, the calculated $I_{cf(weak)}$ is insignificant and does not affect other characteristics. When $\psi_{sf} > 2\phi_B$, $I_{cf(weak)}$ is calculated simply for numerical continuity to strong inversion. Even though $I_{cf(weak)}$ is getting larger than the strong-inversion current, it is not problematic since its effect on I_{WK} is suppressed by the limiting current as discussed in Section 4.2.3. A proper limiting of ψ_{sf}, however, is needed in evaluating the back-surface band bending ψ_{sb} by (4.20) and the average vertical field $\bar{E}_{xf}$ by (4.4). For the ψ_{sb} and $\bar{E}_{xf}$ calculations, the minimum and maximum values of ψ_{sf} are set equal to zero and $2\phi_B$ respectively, which are physically correct. The same limiting is done to ψ_{sb} in evaluating $\bar{E}_{xb}$ by (4.24). Notice finally that the exponential terms involving ψ_{sf} and ψ_{sb} in (4.8) and (4.21) can be extremely large, and can cause a numerical overflow problem in the iterative solution process. To avoid this, ψ_{sf} and ψ_{sb} are constrained in the evaluations of the weak-inversion currents not to exceed fifty times V_{th}.

The next step in the I_{WK} algorithm is the calculation of carrier mobilities at the front and back surfaces using (4.5)

and (4.23). The low-field mobility μ_{n0} in these equations is the model parameter that is commonly used for both the front and back channels. In the contemporary SOI technology, however, the quality of the back $Si-SiO_2$ interface is inferior to that at the front, for example, due to the damage incurred during oxide implantation in SIMOX technology [Izu78]. The back-channel mobility values measured in our test devices, fabricated on SIMOX material, show a large variation between approximately 60 % and 90 % of the front-channel mobilities, depending on the back-surface quality reflected by the calculated interface-states density. This difference is accounted for in this step by forcing a representative 20 % reduction in the calculated back-channel mobility. The effective channel lengths L_{ef} and L_{eb} are then calculated from (4.9) and (4.22). Finally $I_{cf(weak)}$ and $I_{cb(weak)}$ are evaluated by (4.8) and (4.21).

Notice again that these currents are allowed to become much larger than the strong-inversion current for $V_{GfS} > V_{Tf(eff)}$. Limiting currents I^{f}_{LIMIT} and I^{b}_{LIMIT} are defined as discussed in Section 4.2.3 to limit the weak-inversion currents, and I_{WK} is calculated by (4.27). Note here that the possible strong-inversion current at the back channel is represented only by I^{b}_{LIMIT}.

5.2.4 Numerical Techniques

In this section, the numerical techniques, which were chosen to increase the computational efficiency and to alleviate convergence problems of SOISPICE-2, are discussed.

In Fig. 5.2, the calculations of $Q_{b(eff)}$, $V_{DS(sat)}{}^{*}$, and $V_{DS(eff)}$ require iterative procedures, in addition to the loops shown. For these iterations, a simple direct method has been chosen; each system of equations is solved directly, using the solution of the previous iteration as an input. If the new solution is not equal to the previous one within an error tolerance, the new value is returned to the beginning of the iteration loop. Even though this iteration method is not very efficient, it is fast enough for the simple sets of equations alluded to.

However the main loops in Fig. 5.2 involving the V_{LDS} and V_{LDD} calculations are too intensive to be handled by the direct-iteration method. A good candidate for solving this kind of a strongly coupled, implicit set of equations is the secant method, which does not require analytical expressions for function derivatives as does the classical Newton-Raphson method. The secant method [Mcc88], however, has occasional difficulties in convergence, especially when the iterate should remain within a specified interval as in the LDS and LDD iterations on V_{LDS} and V_{LDD}. A hybrid secant-bisection method [Jeo89] has been chosen for these iterations to ease

the convergence problem while maintaining good computational efficiency.

5.2.4.1 Hybrid Secant-Bisection Method

As implied by Fig. 5.2, the new V_{LDD}^* is really an implicit function of the iterate V_{LDD}, the value of which should remain within the interval [0, V_{DS}^*]. The complete set of equations in this iteration can be represented as

$$G(V_{LDD}) = V_{LDD}^*(V_{LDD}) - V_{LDD} = 0 \quad . \tag{5.2}$$

The $V_{LDD}^*(V_{LDD})$ dependence is defined implicitly; it is not given in analytical form as a function of V_{LDD}. The new guess for V_{LDD} is therefore calculated by the secant iteration method, but forced to remain within the interval by bracketing and the bisection method.

In Fig. 5.4, the algorithm for this hybrid secant-bisection method is flowcharted. As shown in Fig. 5.4, if $G_i(V_{LDD}^i) = 0$ is not satisfied, bracketing is first performed to reduce the interval where the iterate V_{LDD}^{i+1} should remain. Next the secant method is used to calculate a new guess V_{LDD}^{i+1}. If V_{LDD}^{i+1} falls outside the specified bracket, the bisection method is invoked to redefine the new guess. The LDS routine utilizes the same method with V_{LDS} as its iterate.

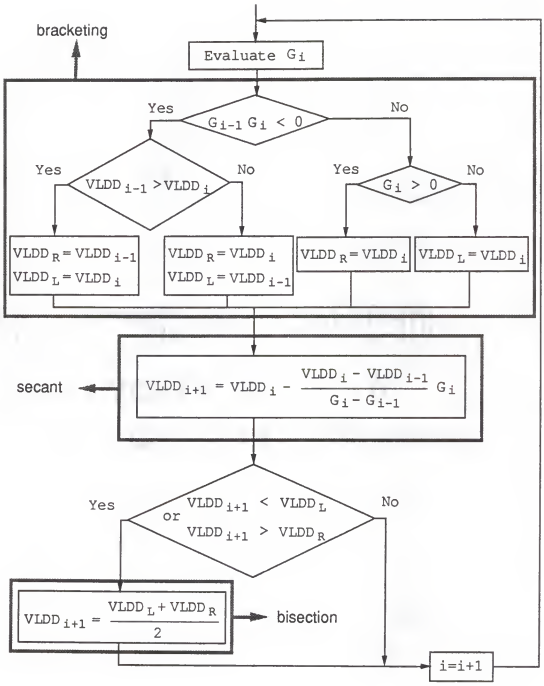


Fig. 5.4 Algorithm of the hybrid secant-bisection method used in the LDD iteration loop.

5.2.4.2 Underflow

A method to avoid numerical underflow in SOISPICE-2 is introduced and described in this section. Similarly to the numerical overflow problem involving the exponential terms in (4.8) and (4.21), which was discussed in Section 5.2.3, an underflow problem can occur in all exponential terms involving negative exponents. For example in the weak-inversion current expressions (4.8) and (4.21), the exponential term involving V_{DS} should be zero for large V_{DS}. However it is numerically nonzero, being a very small number which may not be defined in a given precision. This underflow problem can be resolved by limiting the negative exponent at some value which does not affect the model characteristics. In SOIMOD, this limiting is done by forcing the exponent to always be greater than -50.

5.2.4.3 Numerical Options

To alleviate convergence problems in SOISPICE-2, a minimum shunting conductance GMIN is added to junction currents, as is done in SPICE2. This is not essential, but is expected to ease convergence in simulating large circuits.

The GMIN terms are added to the I_R and I_{Gt} expressions, discussed in Chapter 4 and in Section 5.2.2, as follows:

$$I_R = I_{RO} \left[\exp\left(\frac{V_{BS}}{V_{th}}\right) - 1\right] + \text{GMIN } V_{BS} \qquad (5.2)$$

and

$$I_{Gt} = I_{GtO}\ [1-\exp(\frac{V_{BD}}{V_{th}})] - GMIN\ V_{BD} \quad . \tag{5.3}$$

The value of GMIN can be altered from its default value of $10^{-12}\ \Omega^{-1}$ in the option card of the SOISPICE-2 circuit file. For accurate simulations, for example in device or small circuit simulations, GMIN = 10^{-20} is recommended so as not to affect the model accuracy at all.

Furthermore, the 'PIVTOL' and 'ABSTOL' values [Vla81] in the option card should be chosen differently from their default values (10^{-13} and 10^{-12} A respectively) since the terms involving I_{WK}, I_R, and I_{Gt} are accessing numerically small numbers. PIVTOL is the absolute minimum value for a matrix entry to be accepted as a pivot, and 10^{-20} is recommended. ABSTOL is the absolute current error tolerance of the program, and 10^{-15} is recommended for accurate simulations.

5.3 Demonstration of Simulating Capability

In this section, simulation results are presented to demonstrate the utility of SOISPICE-2 in the design of fully depleted SOI MOSFETs and circuits, focusing on the new features in the model. Simulations of device subthreshold characteristics are demonstrated and compared with the measured data. The effects of the LDS, the LDD, and the

parasitic BJT are simulated and compared with the PISCES simulations in Chapter 3. Comparison of computation times involving various combinations of the new features is given to show the efficiency and limits of the simulator. SOI CMOS circuit (and device) simulations are included, and an example of a rather large circuit (a ring oscillator) simulation is also given.

5.3.1 Subthreshold Characteristics

Figure 5.5 shows the SOISPICE-2-simulated back-surface leakage problem in a 0.8-μm long, 3.6-μm wide, and 0.28-μm thick fully depleted n-channel SOI MOSFET, which was experimentally exemplified in Fig. 4.2. The model parameters DL and DW were assumed equal to 0.1 μm to account for the lateral diffusion of the source and drain. Key model parameters and biases are described in the figure caption. Note that as V_{DS} increases, the off-state leakage increases. This is due to the back-surface DIBL and the concomitant weak-inversion current. The predicted leakage current resulting from the DIBL is in good agreement with the measurement.

Figure 5.6 is another illustration of the back-surface leakage problem in the same device. Measured and simulated subthreshold characteristics are shown for varying back-gate bias. Note the humps in the characteristics that form as V_{GbS} increases (toward the back-channel threshold voltage). The

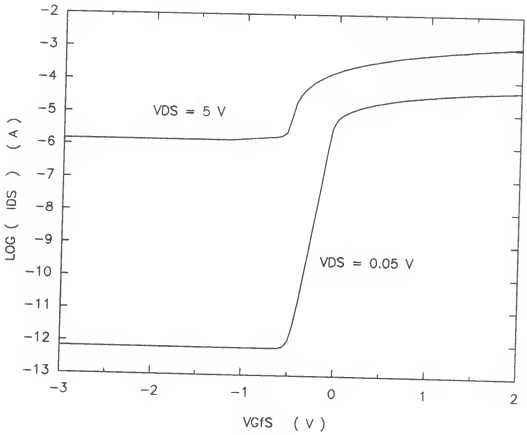
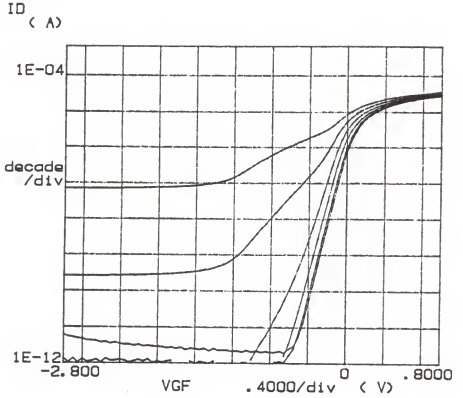
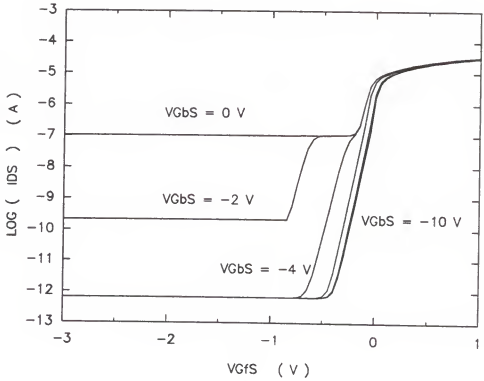


Fig. 5.5 SOISPICE-2-simulated back-channel DIBL leakage of the device in Fig. 4.2. The bias condition is same as in Fig. 4.2; V_{GbS} = -5 V and V_{BS} = 0 V. Key model parameters are NBODY = 8×10^{15} cm^{-3}, N_{LDS} = 3×10^{18} cm^{-3}, NQFF=2×10^{10} cm^{-2}, and NQFB =2.5×10^{11} cm^{-2}.

Fig. 5.6 Subthreshold characteristics of the device in Figs. 4.2 and 5.5 as a function of V_{GbS}.
(a) Measured; (b) SOISPICE-2-simulated.
The humps are caused by the back-channel leakage.


ID
(A)
1E-04
decade
/div
1E-12
-2.800
0
.8000
VGF
.4000/div
(V)


-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
-13
LOG (IDS) (A)
VGbS = 0 V
VGbS = -2 V
VGbS = -4 V
VGbS = -10 V
-3
-2
-1
0
1
VGfS (V)

hump is typically seen in subthreshold characteristics of fully depleted devices, but has not been well explained. Indeed we deduce here that the hump occurs since the back-channel current, which increases as the front-gate bias increases, exceeds the front-channel subthreshold current. This is because the back-channel threshold voltage is a function of the front-gate bias by the front gate-back gate coupling [Lim83]. There is a discrepancy in the shape of the humps between the measurements and the simulations mainly because the back-channel strong-inversion current is represented merely by the fixed limiting current in (4.30). However the trend and levels of the predicted leakage current are in good agreement with the measurements.

5.3.2 Effects of LDS, LDD, and Parasitic BJT

Figure 5.7 shows the SOISPICE-2-predicted influence of the LDS and LDD on the on-state breakdown characteristic of a fully depleted SOI MOSFET. These simulations duplicate those done with PISCES in Chapter 3 (See three versions of device D in Fig. 3.14) for the same device structure. The length and doping of the LDS and LDD were 0.2 μm and 10^{17} cm^{-3} respectively. The effective length of the n^+-source region, L_S, was changed from its default value of 0.5 μm to 20 nm when the LDS was included. The predicted changes in breakdown characteristics are in good agreement with the PISCES simulation results.

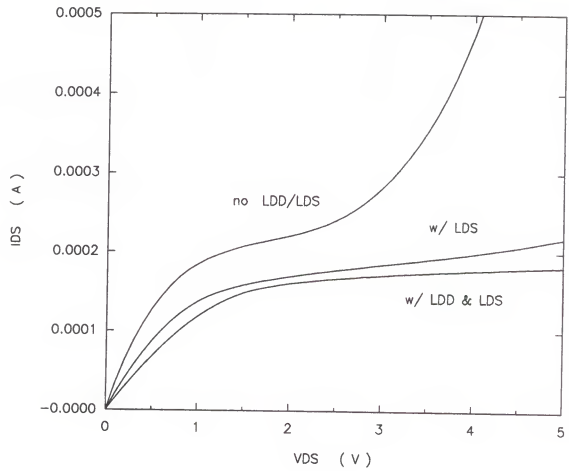


Fig. 5.7 SOISPICE-2-simulated on-state breakdown characteristics of three versions of device D in Fig. 3.14. The same bias condition and device parameters are used.

Figure 5.8 shows the change in the off-state latch characteristics of the same device, with and without the LDS and LDD, as predicted by SOISPICE-2. Comparing these simulations with the corresponding PISCES simulations in Fig. 3.13, we see that the predicted increase in the latch voltage due to the LDS differs significantly. This discrepancy may be caused by the full-depletion limitation of the SOISPICE-2 model. In the off-state, the SOI film could be only partially depleted, and the parasitic BJT current gain could be much lower due to the recombination near the source-body junction area, which was not considered in the model. If this component of recombination were accounted for, the latch voltages predicted in Fig. 5.8 would be higher and would show the snapback behavior as in Fig. 3.13.

Figures 5.9 and 5.10 are SOISPICE-2 simulation results showing the effects of the LDD doping and length on SOI MOSFET DC characteristics. The simulation of the device without an LDD is also included in Figs. 5.9 and 5.10 for comparison. We note that no LDS was included in the simulations. Figure 5.9 shows predicted changes in the I_{DS}-V_{DS} characteristics. The linear-region conductance decreases due to the increased ohmic drop in the LDD region as the LDD doping decreases and the LDD length increases. Notice that the magnitude of the saturation current does not vary significantly with the changes in LDD parameters, but the saturation voltage and saturation-region conductance do.

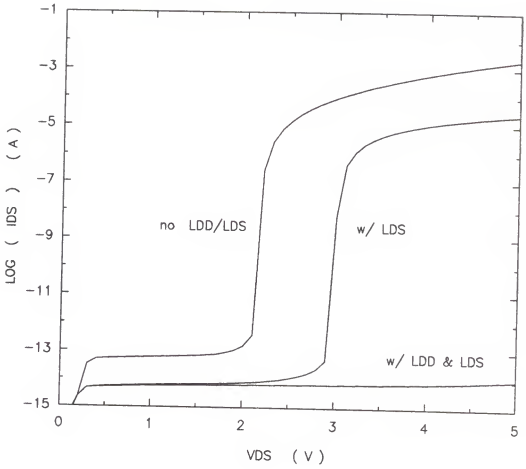


Fig. 5.8 SOISPICE-2-simulated off-state breakdown characteristics of two versions of device D in Fig. 3.13 and another version including both LDS and LDD. The same bias condition and device parameters are used.

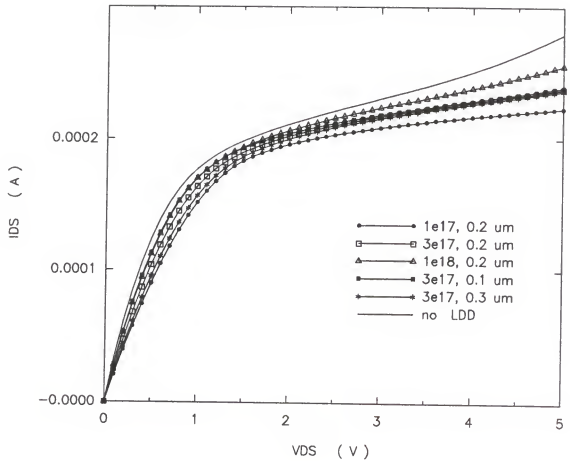


Fig. 5.9 SOISPICE-2-simulated I_{DS}-V_{DS} characteristics as functions of LDD doping and length. (V_{GfS}-V_{Tf}) = 2 V and the body was grounded to monitor I_{Gi}. W = 1 μm, L = 0.5 μm, TOXF = 20 nm, TB = 0.1 μm, and NBODY = $2x10^{16}$ cm^{-3}. No LDS was included.

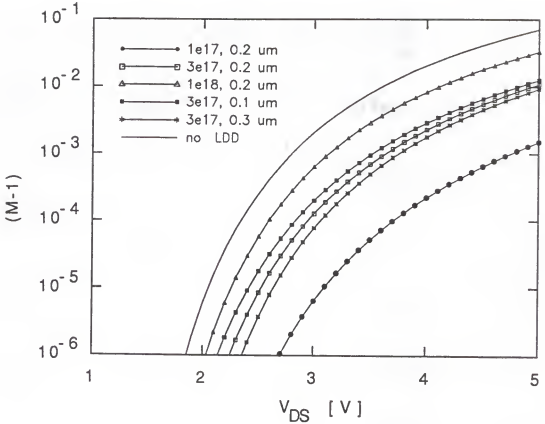
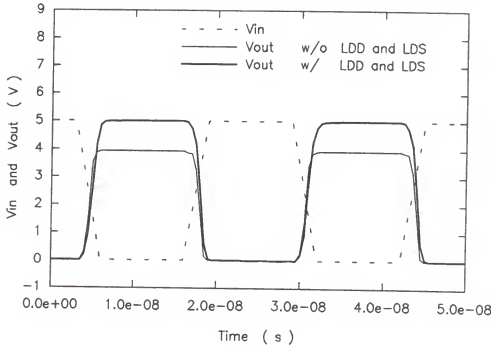


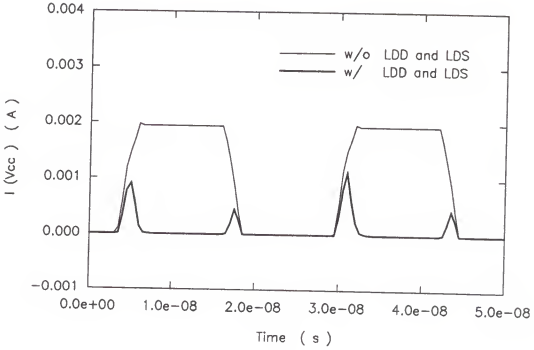
Fig. 5.10 Predicted impact-ionization multiplication factor of the devices in Fig. 5.9 (same symbols).

Figure 5.10 shows the corresponding changes in the impact-ionization multiplication factor, calculated as the predicted body current divided by the drain current. Even though supporting measured data is not available, the predicted trends seem reasonable, and these simulations exemplify well how SOISPICE-2 can be effectively used in the technical design of the fully depleted SOI MOSFET.

In Fig. 5.11, the effects of the LDD and LDS on transient characteristics of an SOI CMOS inverter are simulated. The inverter comprises 0.5-μm n- and p-channel transistors with LDD and LDS regions. The bodies of both n- and p-channel devices were left floating, and the parasitic BJT model was turned on. Model parameters assumed are identical to those in Fig. 5.12 except that BETA for the n-channel device is 2.0×10^6 and TAU0 = 10^{-6}. The predicted transient output-voltage swings and the currents through the supply voltage source are shown in Fig. 5.11, from simulations done with and without the LDS and LDD. There are obvious differences in the simulation results. As discussed in Chapter 3, the n-channel device of the no-LDD/LDS CMOS inverter latches in its off-state with high V_{DS}, and causes unacceptable standby current and power consumption during the half cycle (see Fig. 5.11-(b)). In the other half cycle however, where the n-channel device is on, the p-channel device in the off-state does not latch due to less impact ionization. The output-voltage swing of the inverter is

Fig. 5.11 SOISPICE-2-simulated characteristics of CMOS inverter with and without LDD and LDS. The thinner lines are for the CMOS inverter without LDD and LDS.
(a) output-voltage swings; (b) currents through the supply voltage source V_{cc}.
The LDD/LDS doping and length were $3x10^{17}$ cm^{-3} and 0.2 μm respectively. LS was 20 nm for simulations including LDD and LDS, and 0.5 μm for no LDD/LDS case. The parasitic BJT was turned on.


Vin
Vout w/o LDD and LDS
Vout w/ LDD and LDS
Vin and Vout (V)
9
8
7
6
5
4
3
2
1
0
−1
0.0e+00
1.0e−08
2.0e−08
3.0e−08
4.0e−08
5.0e−08
Time (s)


w/o LDD and LDS
w/ LDD and LDS
I (Vcc) (A)
0.004
0.003
0.002
0.001
0.000
−0.001
0.0e+00
1.0e−08
2.0e−08
3.0e−08
4.0e−08
5.0e−08
Time (s)

reduced concomitantly as shown in Fig. 5.11-(a). The LDD/LDS version of the inverter eliminated the power-consumption problem and recovered the desired full-voltage swing by suppressing the parasitic BJT and hence increasing the latch voltage of the n-channel device above 5 V as exemplified in the simulations in Fig. 5.8, albeit however with an increase in delay time probably due to the reduced current drive.

As mentioned previously, the model does not predict the DC snap-back behavior in the off-state, and therefore the latch voltage of the no-LDS/LDD CMOS inverter is simply determined by the DC off-state breakdown voltage of the n-channel device in this simulation. If the model could predict the DC snap-back, the latch voltage of the circuit might be affected by the turn-off transient of the n-channel device, in analogy to the hysteresis shown in Fig. 3.10.

5.3.3 Computation Time Comparison

Table 5.2 shows SOISPICE-2 computation-time comparison for various combinations of the individual models in DC and transient simulations of a fully depleted n-channel SOI MOSFET and a CMOS inverter. The gate length was 1 μm, and the width was 5 μm for the n-channel MOSFET and 10 μm for the p-channel. Model parameters are identical to those assumed for the simulations in Fig. 5.11. Simulation run times for the MOSFET bodies floating and grounded are also compared. The

TABLE 5.2
SOISPICE-2 RUN-TIME COMPARISONS

Unit : second

Models		n-channel MOSFET V_{DS} sweep		CMOS inverter			
		grounded	floating	grounded body		Floating body	
		DC	DC (*)	DC	TRAN	DC	TRAN (*)
no LDD/LDS	w/o I_{Gi}	1.08	1.25	2.52	3.93	2.65	6.45
	w/ I_{Gi}	1.08	1.65/1.77	2.75	4.17	3.53	8.58/9.35
LDD only	w/o I_{Gi}	2.30	3.10	6.00	8.72	6.45	12.68
	w/ I_{Gi}	2.45	4.87/5.08	6.98	9.67	9.30	17.4/16.8
LDS only	w/o I_{Gi}	2.25	3.08	5.32	7.25	6.30	11.90
	w/ I_{Gi}	2.30	4.48/5.13	5.78	7.58	8.28	16.5/17.9
LDD & LDS	w/o I_{Gi}	6.77	9.67	16.93	16.52	17.13	26.93
	w/ I_{Gi}	7.48	16.5/18.1	19.27	19.90	25.60	48.6/51.6

* Time including the BJT model is given after the slash (/).

computation time was counted on a SUN4 SPARC station with GMIN = 10^{-20}, PIVTOL = 10^{-20}, and ABSTOL = 10^{-15}, which are the commonly used values for all the simulations discussed. For both DC and transient simulations, 50 bias points were simulated.

For the V_{DS} sweep (from 0 V to 5 V) in the n-channel MOSFET simulation, V_{GfS} was 3 V with the predicted $V_{Tf} \cong 0.7$ V. For the CMOS inverter simulation, V_{cc} was 5 V. V_{in} was swept from 0 V to 5 V for DC simulations, and was a pulse (V_{LOW} = 0 V and V_{HIGH} = 5 V) with a 3-ns rise/fall time for transient simulations.

As shown in Table 5.2, the addition of the LDS/LDD is quite expensive in terms of computing time. However adding these new features provides a useful tool for device design of the fully depleted SOI MOSFET through DC simulations of a single device and transient simulations of simple circuits, as evidenced in Fig. 5.11.

To exemplify the large-circuit simulation capability of SOISPICE-2, we use a five-stage SOI CMOS ring oscillator with a NAND-gate input stage (12 transistors). The SOISPICE-2 circuit file is listed in Fig. 12. Note the n-channel and p-channel model cards, which include the model parameter values. The models, as depicted, include the LDS and LDD accountings. Note that GMIN and ABSTOL values are increased from those used in the previous simulations to ease convergence.

```
.WIDTH  IN=80 OUT=80
*VOLTAGE SOURCE TO TURN ON OSCILLATOR:
 VON 1 0 PULSE 0 5 0 5N 5N 1 2
*POWER SUPPLY
 VCC 5 0 5
 VGB 6 0 0
*INPUT NAND GATE:
 SN0 2 1 0 6 10 GN L=2.0E-6 W=10E-6 AD=100P AS=100P
 SP0 4 1 5 6 11 GP L=2.0E-6 W=5E-6 AD=50P AS=50P
 SN1 4 3 2 6 12 GN L=2.0E-6 W=10E-6 AD=100P AS=100P
 SP1 4 3 5 6 13 GP L=2.0E-6 W=5E-6 AD=50P AS=50P
*SECOND STAGE:
 SN2 7 4 0 6 14 GN L=2.0E-6 W=5E-6 AD=50P AS=50P
 SP2 7 4 5 6 15 GP L=2.0E-6 W=5E-6 AD=50P AS=50P
*THIRD STAGE:
 SN3 8 7 0 6 16 GN L=2.0E-6 W=5E-6 AD=50P AS=50P
 SP3 8 7 5 6 17 GP L=2.0E-6 W=5E-6 AD=50P AS=50P
*FOURTH STAGE:
 SN4 9 8 0 6 18 GN L=2.0E-6 W=5E-6 AD=50P AS=50P
 SP4 9 8 5 6 19 GP L=2.0E-6 W=5E-6 AD=50P AS=50P
*FIFTH (FINAL) STAGE:
 SN5 3 9 0 6 20 GN L=2.0E-6 W=5E-6 AD=50P AS=50P
 SP5 3 9 5 6 21 GP L=2.0E-6 W=5E-6 AD=50P AS=50P
*CURRENT SOURCE TO MONITOR BODY POTENTIAL
 IB0 10 0 0
 IB1 11 0 0
 IB2 12 0 0
 IB3 13 0 0
 IB4 14 0 0
 IB5 15 0 0
 IB6 16 0 0
 IB7 17 0 0
 IB8 18 0 0
 IB9 19 0 0
 IB10 20 0 0
 IB11 21 0 0

*MODEL PARAMETERS FOR N-CHANNEL SOI MOSFET
.MODEL GN NMOSOI NSUB=1.0E14 NBODY=2.0E16 NQFF=2E10 NQFB=1E11 TPS=1.0 TPG=-1.0
+ TOXF=.02U TOXB=.4U TB=.1U CGFDO=100p CGFSO=100p CGFBO=50p UO=700.0 THETA=3E-6
+ VSAT=1E7 QSMA=0.2 QSMB=0.4 ZETA=1.0 ETA=1.0 LMOD=1.0 ALPHA=1.0E6 BETA=2.5E6
+ BFACT=0.3 LIMFAC=3 LDS=0.2U LDD=0.2U NLDS=3E17 NDS=5E19 TAU0=1E-7 LS=0.02U

*MODEL PARAMETERS FOR P-CHANNEL SOI MOSFET
.MODEL GN NMOSOI NSUB=1.0E14 NBODY=2.0E16 NQFF=2E10 NQFB=1E11 TPS=-1.0 TPG=-1.0
+ TOXF=.02U TOXB=.4U TB=.1U CGFDO=100p CGFSO=100p CGFBO=50p UO=350.0 THETA=3E-6
+ VSAT=1E7 QSMA=0.2 QSMB=0.4 ZETA=1.0 ETA=1.0 LMOD=1.0 ALPHA=1.0E6 BETA=4.0E6
+ BFACT=0.3 LIMFAC=3 LDS=0.2U LDD=0.2U NLDS=3E17 NDS=5E19 TAU0=1E-7 LS=0.02U

.TRAN 0.1N 15N
.PRINT TRAN V(1) V(9)
.PLOT TRAN V(1) V(9)
.OPTION ACCT LIST NODE LIMPTS=2000 TNOM=25
+ ABSTOL=1E-12 PIVTOL=1E-20 GMIN=1E-15
.END
```

Fig. 5.12 SOISPICE-2 circuit file for simulation of a five-stage SOI CMOS ring oscillator including LDD and LDS regions.

The simulated ring-oscillator output voltage (of the fourth stage) is plotted in Fig. 5.13. The wave form is again compared with that derived from simulating the circuit with no LDD/LDS devices. The change in oscillation frequency is notable. The oscillation frequency in the LDD/LDS version seems to be lower due to the reduced drive current with the included LDD and LDS region. The run time (on a SUN4 SPARC station) was 830 seconds when the LDD and LDS were included, in comparison with 260 seconds when they were not. As discussed, adding both the LDD and LDS is computationally quite expensive. For simulations of large circuits, it may be necessary to eliminate the LDS (outer) loop by approximating the LDS resistance by the extrinsic source resistance RS in Table 5.1.

5.4 Summary

The model developed in Chapter 4 was successfully implemented into SPICE2 creating SOISPICE-2. The algorithm for implementation was discussed in detail, and the numerical techniques involved were described. The effects of the new features in the model were demonstrated by simulations, which generally were in good agreement with corresponding PISCES simulations and/or measurements. The effect of the off-state latch by the parasitic BJT on a CMOS inverter, discussed in Chapter 3, was well predicted by simulation, and the elimination of the latch by incorporating the LDD/LDS was

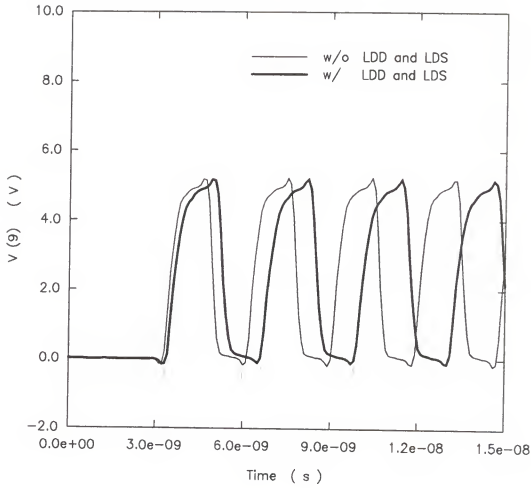


Fig. 5.13 SOISPICE-2-simulated output voltages at node 9 of the five-stage SOI CMOS ring oscillator circuit with and without LDD and LDS. The thinner line is for the circuit without the LDD and LDS.

demonstrated. The computation time of SOISPICE-2 was examined with correspondence to the inclusion of the individual models, and it appeared that adding the LDS and LDD loops is quite expensive in terms of computing time. Exemplary simulations done with SOISPICE-2 suggested that it can be a powerful tool for device and circuit design. DC simulations of fully depleted submicron SOI MOSFETs are physically representative, as are transient simulations of simple circuits such as a CMOS inverter. Simulations of large circuits for design may need some kind of analytical approximation such as the suggested elimination of the LDS (outer) loop.

CHAPTER 6
SUMMARY AND SUGGESTIONS FOR FUTURE WORK

In this dissertation, design issues focussing on the hot-carrier-related device degradation and the floating-body effects, which are the main concerns in contemporary thin-film SOI CMOS technology, have been discussed. A comprehensive understanding of them was attained through analysis by simulations and measurements of submicron fully depleted devices, and a device design to control them was suggested. The floating-body effects, which are difficult to characterize, were intensively analyzed by numerical device simulations. Based on this analysis, a charge-based model for the fully depleted SOI MOSFET that accounts for the subthreshold conduction, the parasitic BJT effects, the effects of the lightly doped source and drain, and the thermal generation current has been developed. The model is physical, and therefore is applicable to fully depleted devices having any channel length. The model was written into the source code of SPICE2 to create the semi-numerical device/circuit simulator SOISPICE-2, which can be effectively used as a design tool for thin-film SOI CMOS ICs. The utility

and the efficiency of SOISPICE-2 were demonstrated through representative simulations.

For future work, we suggest a study of the effects of the LDD, the LDS, and the parasitic BJT on device and circuit performance by simulations with SOISPICE-2. Such a study will also help determine whether more complicated models are required to effectively tradeoff the intensive computation versus simulation accuracy. Considerations of the need to include doping-profile dependence, gate overlap of the LDD and LDS regions, and the parasitic BJT-related body charge should be included in the study.

Work on the model to improve the continuity of the channel conductance (derivative) as well as the current in transition from subthreshold to strong inversion is suggested. This can be done numerically, for example by adopting a cubic polynomial interpolation [Cha87], and/or physically by including a moderate inversion model [Tsi82] which accounts for both the diffusion and drift components of the current. This study will be needed prior to the use of the simulator in analog applications where stricter continuity is required.

A study of SOI MOSFET temperature dependences and their incorporation in the model are worthwhile tasks. The carrier mobilities will be affected, and also the parasitic BJT effect may be more significant at low temperature due to the increased impact ionization and the reduced recombination

rate. The negative drain conductance dI_{DS}/dV_{DS} [Mcd89], which is typically more severe in SOI MOSFETs compared with the bulk counterparts, is assumed to be a thermal effect, and this study could confirm this assumption. Modeling the negative drain conductance will be important for analog circuit simulation.

APPENDIX
STAND-ALONE MODEL ROUTINE

```
C  This program simulates  DC characteristics of fully
C  depleted  floating-body n-channel SOI MOSFET.
C  Only the normal mode operation is allowed; VD ≥ VS.
C  This program is for a VDS sweep as defined by [DO loop
C  900], but other voltage sweeps are possible with a change
C  in [DO loop 900].
C
C  The terminal voltages are defined by VGFSO,VDSO,VGBSO.
C  No contact resistance is considered in this routine.
C
C  This program includes calculation of VBSS, which is the
C  forward bias at source-body junction. Actual floating-body
C  potential is VBSO, which is equal to VBSS+VLDS.
C
C  Unit of length is cm.
C
C  CICH=total channel current=CIST+CIWK
C  CIST=strong inversion current, CIWK=subthreshold current
C  CIT=BJT collector current
c  CIGI=impact ionization current
C  CIGT=thermal generation current
C  CIR=recombination current
C
      implicit double precision (a-h,o-z)
      dimension R(20,20)
      dimension VD(50)
      dimension VLDD(50)
      dimension VS(50)
      dimension VLDS(50)
      dimension VBS(200)
      dimension V(200)
      dimension VBINIT(100)
C
C  Flags indicating linear, saturation, or cutoff;
C  for later charge calculation
C
      LLIN=1
      LSAT=1
C
C  Define output files
```

```
      open(unit=2,file='t.i1',status='unknown')
      open(unit=3,file='t.v1',status='unknown')
      open(unit=4,file='t.q1',status='unknown')
C
C  Initial terminal voltages
C
      VDSO=0.05D0
      VGFSO=3.0D0
      VGBSO=0.0D0
C
C  Flags for various models:
C
      BJT=1.0D0
      XLMOD=1.0D0
      ETA=1.0D0
      ZETA=1.0D0
      ALPHAP=1.0D6
      BETAP=2.0D6
      XLDS=0.2D-4
      XLDD=0.2D-4
C
C  Model parameters:
C
      XL=0.5D-4
      XW=1.0D-4
      TOXF=0.02D-4
      TOXB=0.4D-4
      TB=0.1D-4
      XNBODY=2.0D16
      XNSUB=1E14
      XNLDS=2.0D17
      XNDS=5.0D19
      XLS=0.02D-4
      XMU=700D0
      TAU0=1.0D-7
      XNQFF=2.0D10
      XNQFB=2.0D11
      XLIMFAC=3.0D0
      QSMA=0.2D0
      QSMB=0.4D0
      THETA=3.0D-6
      BFACT=0.4D0
      ABDIFF=QSMA-QSMB
C
C  Basic constants:
      CHARGE=1.6D-19
      EPSSIL=11.7D0*8.85D-14
      XNI=1.4D10
      EG=1.121D0
      VT=0.0259D0
      XNDSEFF=1.0D18
      VSAT=1.0D7
```

```
C
C  Intermediate parameters:
C
C  POLY= 1 for n+poly gate and -1 for p+poly
C
      POLY=1
C
      PHIB=2.0D0*VT*DLOG(XNBODY/XNI)
      COXF=3.9D0*8.85D-14/TOXF
      COXB=3.9D0*8.85D-14/TOXB
      WKF=-(EG/2.0D0+PHIB/2.0D0)
      IF(POLY.LT.0.0D0)THEN
      WKF=EG/2.0D0-PHIB/2.0D0
      ENDIF
      WKB=-(PHIB/2.0D0-VT*DLOG(XNSUB/XNI))
      VFBF=WKF-CHARGE*XNQFF/COXF
      VFBB=WKB-CHARGE*XNQFB/COXB
      VBI=EG/2.0D0+VT*DLOG(XNBODY/XNI)
      VBIS=VBI
      VBID=VBI
      TBBYXL=TB/XL
      QB=-CHARGE*XNBODY*TB
      CB=EPSSIL/TB
      QBBYCB=QB/CB
      CBBYCOB=CB/COXB
      CBBYCOF=CB/COXF
      QBBYCOB=QB/COXB
      QBBYCOF=QB/COXF
C
      BETA=XW*XMU*COXF/2.0D0/XL
      FSAT=XMU/2.0D0/XL/1.0D7
      XALPHA=1.0D0+CBBYCOF/(CBBYCOB+1.0D0)
      XALPHAB=1.0D0+CBBYCOB/(CBBYCOF+1.0D0)
      XLC=TB*DSQRT(0.5D0*CBBYCOF
     &   *(1.0D0+CB/(CB+COXB))/XALPHA)
      XLCB=TB*DSQRT(0.5D0*CBBYCOB
     &   *(1.0D0+CB/(CB+COXF))/XALPHAB)
      XLMODFAC=XLC*XLMOD/XL
      ARG1=0.5D0*THETA/(TB*CBBYCOF)
      XBFACT=BFACT*(2.0-XALPHA)*ARG1
C
      XLEBYXL=1.0D0
      QSHARE=0.0D0
      QBEFFBYCOF=QBBYCOF
C
C  Mobility: 80% of bulk mobility
C
      XMULDSMAJ=92D0+(1360D0-92D0)
     &   /(1.0D0+(XNLDS/1.3D17)**0.91)
      XMULDSMAJ=0.8D0*XMULDSMAJ
      XMULDSMIN=47.7D0+(495D0-47.7D0)
     &   /(1.0D0+(XNLDS/6.3D16)**0.76)
```

```
      XMULDSMIN=0.8D0*XMULDSMIN
      XMUDS=47.7D0+(495D0-47.7D0)/(1.0D0+(XNDS/6.3D16)**0.76)
      XMUDS=0.8D0*XMUDS
C
C  Carrier Lifetimes
C
      CAP=2.0D-31
C
      TAULDS=1.0D0/
     &   ((1.0D0+XNLDS/5.0D16)/TAU0+CAP*XNLDS*XNLDS)
      TAUDS=1.0D0/((1.0D0+XNDS/5.0D16)/TAU0+CAP*XNDS*XNDS)
C
C  Generation Lifitime in body region
C
      TAUG=2.0D0*TAU0/(1.0D0+XNBODY/5.0D16)
C
C  Miscellaneous
C
      RLDD=1/(XW*TB*CHARGE*XNLDS*XMULDSMAJ)
      ESLOPE=CHARGE*XNLDS/EPSSIL
C
C  VDSO is the external terminal voltage.
C  VDS is the internal terminal voltage, which is (VDSO-
C  VLDS). VLDS is the voltage drop at LDS region.
C--------------------------------
C  Start of main voltage sweep
C--------------------------------
      VDSO=-0.1D0
      DO 900 I=1,51
      VDSO=VDSO+0.1D0
C
      LLIN=1
      LSAT=1
C
C  CIGT calculation
C  (Differently from SOIMOD.f, CIGT=f(VDS) is used for
C   simplicity.)
C
      CIGT=CHARGE*XNI*XW*TB*XL/TAUG*(1.0D0-DEXP(-VDSO/VT))
C
C  Initial guess for VLDS
C
      VLDS(1)=0.0D0
      VLDS(2)=VDSO/10.0D0
      XRVLDS=VDSO*0.8D0
      XLVLDS=0.0D0
C--------------------------------
C  Start of LDS routine
C--------------------------------
      DO 880 ID=1,50
      VDS=VDSO-VLDS(ID)
      VGBS=VGBSO-VLDS(ID)
```

```
      VGFS=VGFSO-VLDS(ID)
C
C  Threshold voltage calculation
C
      CAP1=1.0D0/(1.0D0+CBBYCOB)
      PSBLONG=(VGBS-VFBB+0.5D0*QBBYCOB+CBBYCOB*PHIB)*CAP1
      IF(PSBLONG.LT.0.0D0)PSBLONG=0.0D0
      IF(PSBLONG.GT.PHIB)PSBLONG=PHIB
      PSB=PSBLONG
      IF(ZETA.EQ.0.0D0)GOTO 16
      IF(XLDS.GT.0.0D0)THEN
        VBIS=VT*DLOG(XNLDS*XNBODY/XNI/XNI)
      ENDIF
      IF(XLDD.GT.0.0D0)THEN
        VBID=VT*DLOG(XNLDS*XNBODY/XNI/XNI)
      ENDIF
C
      DO 10 IA=1,30
        PSBOLD=PSB
        PARTS=XNLDS/(XNLDS+XNBODY)
        PARTD=PARTS
        IF(XLDS.LE.0.0D0)PARTS=1.0D0
        IF(XLDD.LE.0.0D0)PARTD=1.0D0
        ROOTETBS=ZETA*
     &    DSQRT(0.5D0*CHARGE*XNBODY/EPSSIL*(VBIS-PSB)*PARTS)
        ROOTETBD=ZETA*
     &    DSQRT(0.5D0*CHARGE*XNBODY/EPSSIL*(VBID-PSB)*PARTD)
        ETBS=ROOTETBS+(ABDIFF*(VGBS-VFBB)-QSMA*PSB
     &    +QSMB*(VBIS*PARTS+(1.0D0-PARTS)*PSB))*COXB/EPSSIL
        ETBD=ROOTETBD+(ABDIFF*(VGBS-VFBB)-QSMA*PSB
     &    +QSMB*(VBID*PARTD+(1.0D0-PARTD)*PSB))*COXB/EPSSIL
C
        DS=(VBIS-PSB)/ETBS*PARTS
        DD=(VBID-PSB)/ETBD*PARTD
        DS=DMIN1(0.7D0*XL,DS)
        DD=DMIN1(0.7D0*XL,DD)
        IF(ETBS.LE.0.0D0.AND.ETBD.LE.0.0D0)THEN
          QSHARE=0.0D0
        ELSEIF(ETBD.LE.0.0D0)THEN
          QSHARE=0.5D0*DS/XL
        ELSEIF(ETBS.LE.0.0D0)THEN
          QSHARE=0.5D0*DD/XL
        ELSE
          QSHARE=0.5D0*(DS+DD)/XL
        ENDIF
C
        PSB=PSBLONG-0.5D0*QSHARE*QBBYCOB*CAP1
        IF(PSB.GT.PHIB)PSB=PHIB
        IF(PSB.GT.DMIN1(VBIS,VBID))PSB=DMIN1(VBIS,VBID)
        IF(ABS(PSB-PSBOLD).LE.1.0D-6)GOTO 13
   10 CONTINUE
C
```

```
   13 QBEFFBYCOF=QBBYCOF*(1.0D0-QSHARE)
   16 VTFO=VFBF+(1.0D0+CBBYCOF)*PHIB-0.5D0*QBEFFBYCOF
     &   -CBBYCOF*PSB
      VTFF=VTFO
      PSIB=PSB
C
C  Initial guess for floating-body potential
C
      IF(I.EQ.2)THEN
        VBS(1)=VBINIT(1)
        VBS(2)=VBS(1)+0.01D0
        GOTO 17
      ENDIF
      IF(I.GT.2)THEN
        VBS(1)=VBINIT(I-2)
        VBS(2)=VBINIT(I-1)
      IF(VBS(1).EQ.VBS(2))VBS(2)=VBS(1)+0.01D0
        GOTO 17
      ENDIF
C
      VBS(1)=0.0D0
      VBS(2)=1.0D0
C
   17 CONTINUE
C
      DO 850 J=1,200
C
C  Initial guess for VLDD, which is equal to (VDS-VLDD).
C
      VLDD(1)=VDS*0.0D0
      VLDD(2)=VDS*0.4D0
      XLVLDD=0.0D0
      XRVLDD=VDS*0.8D0
C--------------------------------
C  Start of LDD routine
C--------------------------------
      DO 500 IB=1,50
        IF(XLDD.LE.0.0D0)THEN
          VLDD(IB)=0.0D0
        ENDIF
        VDSS=VDS-VLDD(IB)
        DELVTF=-ETA*CBBYCOF*TBBYXL*TBBYXL*(2.0D0-CAP1)*VDSS
        VTFF=VTFO+DELVTF
        VGFST=VGFS-VTFF
        V01=VGFST/XALPHA
C
C  IWK,Le,Leb calculation
C  For current calculation, SPSIF is allowed to increase over
C  PHIB.
C
        SPSIF=PHIB+V01
        PSIF=SPSIF
```

```
        IF(PSIF.GT.PHIB)PSIF=PHIB
        IF(PSIF.LT.0.0D0)PSIF=0.0D0
        SPSIB=CAP1*(VGBS-VFBB+0.5D0*QBEFFBYCOF*COXF/COXB)
     &    +(1.0D0-CAP1)*(PSIF-DELVTF/(2.0D0-CAP1)/CBBYCOF)
        PSIB=SPSIB
        IF(PSIB.GT.PHIB)PSIB=PHIB
        IF(PSIB.LT.0.0D0)PSIB=0.0D0
C
        XEXF=(PSIF-PSIB)/TB-0.5D0*QBEFFBYCOF*COXF/EPSSIL
        IF(PSIB.GT.PSIF)THEN
          XEXF=-0.5D0*QBEFFBYCOF*COXF/EPSSIL
        ENDIF
        XMOBREF=1.0D0/(1.0D0+THETA*XEXF)
        XMUEFF=XMU*XMOBREF
        XEXB=(PSIB-PSIF)/TB-0.5D0*QBEFFBYCOF*COXF/EPSSIL
        IF(PSIF.GT.PSIB)THEN
          XEXB=-0.5D0*QBEFFBYCOF*COXF/EPSSIL
        ENDIF
C
C  Consider 20% reduction in back-channel mobility here
C
        XMOBREFB=1.0D0/(1.0D0+THETA*XEXB)*0.8D0
        XMUEFFB=XMU*XMOBREFB
        TEMP1=XMOBREF*FSAT*VDSS*XL/XLC
        XLEBYXL=1.0D0-XLMODFAC
     &    *DLOG(TEMP1+DSQRT(1.0D0+TEMP1*TEMP1))
C
        IF(XLEBYXL.LT.1.0D-3)THEN
          XLEBYXL=1.0D-3
          print *, 'Le=0 during iteration at VDS=',VDSO
        ENDIF
C  Avoid possible overflow
        IF(SPSIF.GT.5.0D1*VT)SPSIF=5.0D1*VT
C  Avoid possible underflow
        IF(SPSIF.LT.-5.0D1*VT)SPSIF=-5.0D1*VT
        SARG=0.0D0
        STERM=VDSS/VT
        IF(STERM.LT.5.0D1)  SARG=DEXP(-STERM)
C
        CIWKF=XW/XL/XLEBYXL*VT*VT*XMUEFF*CHARGE*XNI*XNI
     &    /XNBODY/XEXF*DEXP(SPSIF/VT)*(1.0D0-SARG)
        TEMP2=XMOBREFB*FSAT*VDSS*XL/XLCB
        XLEBBYXL=1.0D0-XLMODFAC*XLCB/XLC
     &    *DLOG(TEMP2+DSQRT(1.0D0+TEMP2*TEMP2))
C
        IF(XLEBBYXL.LT.1.0D-3)THEN
          XLEBBYXL=1.0D-3
          print *, 'Leb=0 during iteration at VDS=',VDSO
        ENDIF
C  Avoid possible overflow
        IF(SPSIB.GT.5.0D1*VT)SPSIB=5.0D1*VT
C  Avoid possible underflow
```

```
          IF(SPSIB.LT.-5.0D1*VT)SPSIB=-5.0D1*VT
          CIWKB=XW/XL/XLEBBYXL*VT*VT*XMUEFFB*CHARGE*XNI*XNI
     &     /XNBODY/XEXB*DEXP(SPSIB/VT)*(1.0D0-SARG)
C
C     Limiting currents
C     (CIFLIM for front channel, CIBLIM for back channel)
C     PSIF=PHIB for CIFLIM, and PSIB=PHIB for CIBLIM)
C
          TPSIB=SPSIB-(1.0D0-CAP1)*(PSIF-PHIB)
          IF(TPSIB.GT.PHIB)TPSIB=PHIB
          IF(TPSIB.LT.0.0D0)TPSIB=0.0D0
          TEXF=(PHIB-TPSIB)/TB-0.5D0*QBEFFBYCOF*COXF/EPSSIL
          IF(TPSIB.GT.PHIB)THEN
            TEXF=-0.5D0*QBEFFBYCOF*COXF/EPSSIL
          ENDIF
          TMOBREF=1.0D0/(1.0D0+THETA*TEXF)
          TMUEFF=XMU*TMOBREF
          TEMP1=TMOBREF*FSAT*VDSS*XL/XLC
          TLEBYXL=1.0D0-XLMODFAC
     &      *DLOG(TEMP1+DSQRT(1.0D0+TEMP1*TEMP1))
          IF(TLEBYXL.LT.1.0D-3) THEN
            TLEBYXL=1.0D-3
          ENDIF
          CIFLIM=0.5D0*COXF*TMUEFF*XW/XL/TLEBYXL
     &      *XLIMFAC*XLIMFAC*VT*VT*(1.0D0-SARG)
C
          TPSIF=1.0D0/(1.0D0+CBBYCOF)*(VGFS-VFBF
     &      +0.5D0*QBEFFBYCOF)+CBBYCOF/(CBBYCOF+1)
     &      *(PHIB-DELVTF/(2.0D0-CAP1)/CBBYCOF)
          IF(TPSIF.GT.PHIB)TPSIF=PHIB
          IF(TPSIF.LT.0.0D0)TPSIF=0.0D0
          TEXB=(PHIB-TPSIF)/TB-0.5D0*QBEFFBYCOF*COXF/EPSSIL
          IF(TPSIF.GT.PHIB)THEN
            TEXB=-0.5D0*QBEFFBYCOF*COXF/EPSSIL
          ENDIF
C
C   Consider 20% reduction in back-channel mobility here
C
          TMOBREFB=1.0D0/(1.0D0+THETA*TEXB)*0.8D0
          TMUEFFB=XMU*TMOBREFB
          TEMP2=TMOBREFB*FSAT*VDSS*XL/XLCB
          TLEBBYXL=1.0D0-XLMODFAC*XLCB/XLC
     &      *DLOG(TEMP2+DSQRT(1.0D0+TEMP2*TEMP2))
          IF(TLEBBYXL.LT.1.0D-3) THEN
            TLEBBYXL=1.0D-3
          ENDIF
C
          CIBLIM=0.5D0*COXB*TMUEFFB*XW/XL/TLEBBYXL
     &      *XLIMFAC*XLIMFAC*VT*VT*(1.0D0-SARG)
C
          IF(CIFLIM.LE.0.0D0.OR.CIBLIM.LE.0.0D0)THEN
            CIWKF=0.0D0
```

```
          CIWKB=0.0D0
          GOTO 19
        ENDIF
        CIWKF=CIWKF*CIFLIM/(CIWKF+CIFLIM)
        CIWKB=CIWKB*CIBLIM/(CIWKB+CIBLIM)
   19   CIWK=CIWKF+CIWKB
C
      CIST=0.0D0
      VDSAT0=0.0D0
      VDSAT=0.0D0
C
      IF(VGFST.LE.0.0D0)GOTO39
C
C  Calculation of VDSAT0 for strong inversion, which is the
C  value of VDSS at the onset of saturation.
C  For subthreshold, VDSAT0=0
C
      XLEBYXL=1.0D0
      DELVTF0=0.0D0
      DO 20 JA=1,30
        DELVTFOLD=DELVTF0
        VGFST0=VGFS-VTFO-DELVTF0
        V010=VGFST0/XALPHA
        XMOBRED0=1.0D0/(1.0D0+ARG1*(VGFS-VTFO+DELVTF0
     &     -QBEFFBYCOF+2.0D0*CBBYCOF*(PHIB-PSIB)))
        XBMU0=XBFACT*XMOBRED0
        TEMP1=1.0D0+V010*(XBMU0+FSAT*XMOBRED0)
        VDSAT0=V010/(TEMP1*(0.5D0+DSQRT(0.25D0-XBMU0*V010
     &     /(TEMP1*TEMP1))))
        DELVTF0=-ETA*CBBYCOF*TBBYXL*TBBYXL
     &     *(2.0D0-CAP1)*VDSAT0
        IF(ABS(DELVTFOLD-DELVTF0).LE.1.0D-6)GOTO 23
   20 CONTINUE
   23 VDSAT0=DMAX1(VDSAT0,0.0D0)
C
C  Use iteration to numerically determine
C  VDS(eff)=VDSAT=f(VDSS,Le)  for saturation.
C  This involves calculation of channel mobility, channel
C  current. For subthreshold, VDSAT=0
C
      XMOBRED=1.0D0/(1.0D0+ARG1*(VGFS-VTFO+DELVTF
     &  -QBEFFBYCOF+2.0D0*CBBYCOF*(PHIB-PSIB)))
      XBMU=XBFACT*XMOBRED
C  Set initial value for VDSAT
      VDSAT=VDSAT0
C
      IF(VDSS.LE.VDSAT0)GOTO 33
C
      IF(XLMODFAC.LE.0.0D0)GOTO 36
C
      DO 30 JB=1,30
        VDSATOLD=VDSAT
```

```
          XMOBREF=XMOBRED/(1.0D0-XBMU*VDSAT)
          ARG2=(VDSS-VDSAT)*XMOBREF*FSAT/XLMODFAC
          XLEBYXL=1.0D0-XLMODFAC
     &      *DLOG(ARG2+DSQRT(1.0D0+ARG2*ARG2))
C
          IF(XLEBYXL.LT.1.0D-3)THEN
            print *, '30: Le=0 during iteration at VDS=',VDSO
            XLEBYXL=1.0D-3
          ENDIF
C
          ARG3=1.0D0+V01*(XBMU+FSAT*XMOBREF/XLEBYXL)
          VDSAT=V01/(ARG3*(0.5D0+DSQRT(0.25D0-XBMU*V01/
     &      (ARG3*ARG3))))
          IF(ABS(VDSAT-VDSATOLD).LE.1.0D-6)GOTO 36
    30    CONTINUE
C
C   Triode region
C
    33    LLIN=0
          LSAT=1
          VL1=V01-VDSS
          XMOBREF=XMOBRED/(1.0D0-XBMU*VDSS)
          ARGV=V01*V01-VL1*VL1
          DENOMC=1.0D0+FSAT*XMOBREF*VDSS
          CIST=BETA*XMOBREF*XALPHA*ARGV/DENOMC
          GOTO 39
C
C   Saturation region
C
    36    VDSAT=DMAX1(VDSAT,0.0D0)
          LSAT=0
          LLIN=1
          VL1=V01-VDSAT
          XMOBREF=XMOBRED/(1.0D0-XBMU*VDSAT)
          ARGV=V01*V01-VL1*VL1
          DENOMC=1.0D0+FSAT*XMOBREF*VDSAT/XLEBYXL
          CIST=BETA*XMOBREF*XALPHA*ARGV/(DENOMC*XLEBYXL)
C
    39    CONTINUE
C
C   Calculation of total channel current
C
          CICH=CIWK+CIST
C
C   Calculatin of drain max. field Emax
C
          XEM=0.0D0
          IF(VDSS.GE.VDSAT) XEM=(VDSS-VDSAT)/XLC
C
C   BJT Current
C
          CIT=0.0D0
```

```
          IF(BJT.LE.0.0D0)GOTO 43
          IF(VDSO.EQ.0.0D0)GOTO 43
          IF(VBS(J).LE.0.0D0)GOTO 43
          QP=(XL*XLEBYXL)
     &      *(XNBODY+0.5D0*XNI*DEXP(0.5D0*VBS(J)/VT))
          CIT=CHARGE*XW*TB*XNI*XNI*XMU*XMOBREF*VT/QP
     &      *(DEXP(VBS(J)/VT)-1.0D0)
          IF(CIT.LT.0.0D0) CIT=0.0D0
   43 CONTINUE
C
C  VLDD Calculation
C
       CI=CICH+CIT
       IF(XLDD.LE.0.0D0)THEN
         VLDDD=0.0D0
         GOTO 46
       ENDIF
       IF(XEM.LE.CI*RLDD)THEN
         VLDDD=CI*RLDD*XLDD
       ELSE IF((XEM-CI*RLDD).LE.ESLOPE*XLDD)THEN
         VLDDD=0.5D0*(XEM-CI*RLDD)**2/ESLOPE+CI*RLDD*XLDD
       ELSE
         VLDDD=0.5D0*XLDD*(2.0D0*XEM-ESLOPE*XLDD)
       ENDIF
   46 CONTINUE
C
C  Hybrid secant-bisection method
C  Find the next guess for VLDD and/or
C  determine the previous solution is acceptable
C
       VD(IB)=VLDD(IB)-VLDDD
       IF(ABS(VD(IB)).LE.1.0D-6)THEN
         GOTO 503
       ENDIF
       IF(IB.LT.2)GOTO 500
         TEMP=VD(IB)-VD(IB-1)
         IF(ABS(TEMP).EQ.0.0D0)THEN
           PRINT*,'divide by zero at 500'
           goto 9999
         ENDIF
         IF(VD(IB-1)*VD(IB).LT.0)THEN
           XLVLDD=VLDD(IB-1)
           XRVLDD=VLDD(IB)
         IF(VLDD(IB).LT.VLDD(IB-1))THEN
           XLVLDD=VLDD(IB)
           XRVLDD=VLDD(IB-1)
         ENDIF
         ELSEIF(VD(IB).GT.0.0D0)THEN
           XRVLDD=VLDD(IB)
         ELSE
           XLVLDD=VLDD(IB)
         ENDIF
```

```
          VLDD(IB+1)=(VD(IB)*VLDD(IB-1)-VD(IB-1)*VLDD(IB))
     &       /(VD(IB)-VD(IB-1))
          IF(VLDD(IB+1).LT.XLVLDD.OR.VLDD(IB+1).GT.XRVLDD)THEN
            VLDD(IB+1)=(XLVLDD+XRVLDD)/2.0D0
          ENDIF
  500 CONTINUE
  503 CONTINUE
C
C  VDSS=VDS-VLDDD now.
C
C  Impact ionization current
C
       CIGI=0.0D0
C
       IF(VDSO.EQ.0)GOTO 659
       IF(VDSS.LE.VDSAT)GOTO 659
       IF((ALPHAP.EQ.0.0D0).OR.(BETAP.EQ.0.0D0))GOTO 659
C
C  Avoid underflow
       GIARG=0.0D0
       TERMGI=BETAP/XEM
       IF(TERMGI.LT.5.0D1) GIARG=DEXP(-TERMGI)
C
       XMULT1=ALPHAP/BETAP*XLC*XEM*GIARG
       XMULT2=0.0D0
       IF(XLDD.LE.0.0D00)GOTO 656
       FACT=XEM-ESLOPE*XLDD
       IF(XEM.LT.5.0D-3*BETAP)XEM=5.0D-3*BETAP
       IF(FACT.LT.5.0D-3*BETAP)FACT=5.0D-3*BETAP
C  Romberg integration to calculate multiplication in LDD
C  region
       H=XEM-FACT
       R(1,1)=0.5D0*H*(DEXP(-BETAP/FACT)+DEXP(-BETAP/XEM))
       IF(R(1,1).EQ.0.0D0)GOTO 656
       L=1
       DO 650 LA=2,15
         H=0.5D0*H
         L=L+L
         SUM=0.0D0
         DO 600 LB=1,L-1,2
           TEMP=FACT+DREAL(LB)*H
           SUM=SUM+DEXP(-BETAP/TEMP)
  600    CONTINUE
         R(LA,1)=0.5D0*R(LA-1,1)+H*SUM
         M=1
         DO 610 LC=2,LA
           M=4*M
           R(LA,LC)=R(LA,LC-1)+(R(LA,LC-1)
     &       -R(LA-1,LC-1))/DREAL(M-1)
        IF(DABS((R(LA,LC)-R(LA,LC-1))/R(LA,LC)).LT.1.0D-6)THEN
          GOTO 653
        ENDIF
```

```
  610   CONTINUE
  650 CONTINUE
C
  653 CONTINUE
      XMULT2=ALPHAP/ESLOPE*R(LA,LC)
  656 XMULT=XMULT1+XMULT2
C
      CIGI=XMULT*(CICH+CIT)
C
  659 CONTINUE
C
C  Recombination current
C
      IF(XLDS.LE.0.0D0)GOTO 710
      XEP=(CICH+CIT)*RLDD
      TEMP1=XEP*XEP+4.0D0*VT/(XMULDSMIN*TAULDS)
      XM1=0.5D0*(XEP+DSQRT(TEMP1))/VT
      XM2=0.5D0*(XEP-DSQRT(TEMP1))/VT
      TEMP=DEXP(2.0D0*XLS/DSQRT(XMUDS*VT*TAUDS))
      XK=DSQRT(XMUDS*VT/TAUDS)*XNLDS/XNDSEFF
     &  *(TEMP+1.0D0)/(TEMP-1.0D0)
      XC=(-XMULDSMIN*VT*XM1+XMULDSMIN*XEP-XK)
     &  *DEXP((XM1-XM2)*XLDS)
     &  /(XMULDSMIN*VT*XM2-XMULDSMIN*XEP+XK)
      TEMP5=XMULDSMIN*(-VT*(XM1+XC*XM2)/(1.0D0+XC)+XEP)
      CIRO=TEMP5*CHARGE*XW*TB*XNI*XNI/XNLDS
      GOTO 720
  710 CONTINUE
      TEMP=DEXP(2.0D0*XLS/DSQRT(XMUDS*VT*TAUDS))
      CIRO=CHARGE*XW*TB*XNI*XNI/XNDSEFF*DSQRT(XMUDS*VT/TAUDS)
     &  *(TEMP+1.0D0)/(TEMP-1.0D0)
  720 CONTINUE
C  Avoid underflow
      RTERM=VBS(J)/VT
      IF(RTERM.LT.-5.0D1) RTERM=-5.0D1
C
      CIR=CIRO*(DEXP(RTERM)-1.0D0)
      IF(CIR.LT.0.0D0) CIR=0.0D0
C
C  VBS calculation here
C  Secant method
C
C     VBS=VT*DLOG((CIGI+CIGT)/CIRO+1.0D0)
      V(J)=VBS(J)-VT*DLOG((CIGI+CIGT)/CIRO+1.0D0)
      IF(ABS(V(J)).LE.1.0D-4)THEN
        VBSS=VBS(J)
        GOTO 853
      ENDIF
      IF(J.GE.2.0D0)THEN
        TEMP=V(J)-V(J-1)
        IF(ABS(TEMP).EQ.0.0D0)THEN
          PRINT*,'divide by zero at 850'
```

```
          goto 9999
        ENDIF
        VBS(J+1)=(V(J)*VBS(J-1)-V(J-1)*VBS(J))
     &     /(V(J)-V(J-1))
       ENDIF
  850 CONTINUE
  853 CONTINUE
C
      CI=CICH+CIT
C
C  VLDS calculation here
C  Hybrid secant-bisection method
C
      VS(ID)=VLDS(ID)-CI*RLDD*XLDS
      IF(ABS(VS(ID)).LE.1.0D-4)THEN
        VLDSS=VLDS(ID)
        GOTO 883
      ENDIF
      IF(ID.LT.2)GOTO 880
      TEMP=VS(ID)-VS(ID-1)
      IF(ABS(TEMP).EQ.0.0D0)THEN
        PRINT*,'divide by zero at 880'
        GOTO 9999
      ENDIF
      IF(VS(ID-1)*VS(ID).LT.0)THEN
        XLVLDS=VLDS(ID-1)
        XRVLDS=VLDS(ID)
        IF(VLDS(ID).LT.VLDS(ID-1))THEN
          XLVLDS=VLDS(ID)
          XRVLDS=VLDS(ID-1)
        ENDIF
      ELSEIF(VS(ID).GT.0.0D0)THEN
        XRVLDS=VLDS(ID)
      ELSE
        XLVLDS=VLDS(ID)
      ENDIF
      VLDS(ID+1)=(VS(ID)*VLDS(ID-1)-VS(ID-1)*VLDS(ID))
     &  /(VS(ID)-VS(ID-1))
      IF(VLDS(ID+1).LT.XLVLDS.OR.VLDS(ID+1).GT.XRVLDS)THEN
        VLDS(ID+1)=(XLVLDS+XRVLDS)/2.0D0
      ENDIF
  880 CONTINUE
  883 CONTINUE
C
      VBSO=VBSS+VLDSS
C
C  Now VDSS=VDSO-VLDD-VLDS and VBSO is the voltage
C  between external source and floating body.
C
C-----------------------------------------
C  COMMON BLOCK FOR CHARGE CALCULATIONS
C-----------------------------------------
```

```
C  QD=charge related to drain
C  QGF=charge related to front gate
C  QGB=charge related to back gate
C  QBY=charge related to body
C  QS=charge related to source=QN-QD
C
 1000 CONTINUE
C
      WL=XL*XW
      DELQB=WL*COXF*(QBBYCOF-QBEFFBYCOF)
      QDQSH=-0.5D0*DELQB
      QNQSH=-DELQB
C
      IF(LLIN.EQ.0)GOTO 2000
      IF(LSAT.EQ.0)GOTO 3000
C
C  charge components for below-threshold
C
      XLE=XL*XLEBYXL
      DELL=XL-XLE
      ARGHY=DELL/XLC
      CFUN=0.5D0*(DEXP(ARGHY)+DEXP(-ARGHY))
      ARGQG=ARGL*ARGL*(CFUN-1.0D0)/(FSAT*XMOBREF)
C
      QGF=WL*COXF*(VGFS-WKF-PSIF-ARGQG)
c
      QDETA=ETA*WL*CB*TBBYXL*TBBYXL*VDSS
     &   *(XLEBYXL+XLEBBYXL)
c
      QD=QDQSH+QDETA
      QN=QNQSH+QDETA
      QBY=WL*QB
      QGB=-(QN+QGF+QBY+WL*(XNQFF+XNQFB))
      GOTO 9500
C
C  charge components for triode region
C
 2000 CONTINUE
      DNMGF=12.0D0*(VGFST-0.5D0*XALPHA*VDSS)
      ARGS=1.0D0+FSAT*XMOBREF*VDSS
C
      QGF=WL*COXF*(VGFS-WKF-PHIB-0.5D0*VDSS
     &   +VDSS*VDSS*ARGS*XALPHA/DNMGF)
C
      QDETA=ETA*WL*CB*TBBYXL*TBBYXL*VDSS
     &   *(XLEBYXL+XLEBBYXL)
c
      QBY=WL*QB
      IF(VDSS.LE.1.0D-9)GOTO 2002
      ARGU=VGFST/(XALPHA*VDSS)
      ARGZ=ARGU
      IF(FSAT.NE.0.0D0)ARGZ=ARGU-0.5D0*CIST*FSAT
```

```
     &   /(BETA*XALPHA*VDSS)
         TZM1=2.0D0*ARGZ-1.0D0
         XFACTD=(-ARGZ+2.0D0/3.0D0)/TZM1
         QN=-WL*COXF*VGFST*(XFACTD+ARGU)/ARGU+QNQSH+QDETA
C
         ZFACT=(-4.0D0*ARGZ*ARGZ/3.0D0+1.5D0*ARGZ-0.4D0)
     &   /(TZM1*TZM1)
         QD=-WL*COXF*VGFST*(ZFACT+0.5D0*ARGU)/ARGU+QDQSH+QDETA
         QGB=-(QN+QGF+QBY+WL*(XNQFF+XNQFB))
         GOTO 9500
C
C  DRAIN CHARGE FOR VDSS=0; EVALUATED IN THE LIMIT
C
 2002 CONTINUE
         QN=-WL*COXF*VGFST+QNQSH+QDETA
         QD=0.5D0*QN+QDQSH+QDETA
         QGB=-(QN+QGF+QBY+WL*(XNQFF+XNQFB))
         GOTO 9500
C
C  charge components for saturation region
C
 3000 CONTINUE
         XLE=XL*XLEBYXL
         DELL=XL-XLE
         WLE=XLE*XW
         DNMGF=12.0D0*(VGFST-0.5D0*XALPHA*VDSAT)
         ARGS=1.0D0+(FSAT*XMOBREF*VDSAT/XLEBYXL)
C
         QGF=WLE*COXF*(VGFS-WKF-PHIB-0.5D0*VDSAT+
        &   VDSAT*VDSAT*ARGS*XALPHA/DNMGF)
C
         QDETA=ETA*WL*CB*TBBYXL*TBBYXL*VDSS
        &   *(XLEBYXL+XLEBBYXL)
C
         QBY=WL*QB
         IF(DELL.EQ.0.0D0)GOTO 3002
         ARGHY=DELL/XLC
         CFUN=0.5D0*(DEXP(ARGHY)+DEXP(-ARGHY))
         XP=XLC*XLC*(CFUN-1.0D0)/(FSAT*XMOBREF*XL)
         QGFS=XW*COXF*(DELL*(VGFS-WKF-PHIB-VDSAT)-XP)
         QGF=QGF+QGFS
C
 3002 ARGU=VGFST/(XALPHA*VDSAT)
         ARGZ=ARGU
         IF(FSAT.NE.0.0D0)  ARGZ=ARGU-0.5D0*CIST*FSAT/
        &   (BETA*XALPHA*VDSAT)
         TZM1=2.0D0*ARGZ-1.0D0
         XFACTD=(-ARGZ+2.0D0/3.0D0)/TZM1
         QN=-WLE*COXF*VGFST*(XFACTD+ARGU)/ARGU+QNQSH
C
         QCFLE=-COXF*(VGFST-XALPHA*VDSAT)
         QNS=XW*DELL*QCFLE
```

```
      QN=QN+QNS+QDETA
C
      ZFACT=(-4.0D0*ARGZ*ARGZ/3.0D0+1.5D0*ARGZ-0.4D0)
     &   /(TZM1*TZM1)
      QD=-WLE*COXF*VGFST*(ZFACT+0.5D0*ARGU)/ARGU+QDQSH
      QDS=0.5D0*XW*QCFLE*(XL*XL-XLE*XLE)/XL
      QD=QD+QDS+QDETA
      QGB=-(QN+QGF+QBY+WL*(XNQFF+XNQFB))
      GOTO 9500
C
 9500 CONTINUE
C
C  CID=total drain current
      CID=CICH+CIT+CIR
C
      write(2,77) VDSO,CID,CIST,CIWKF,CIWKB,CIT
      write(3,77) VDSO,VBSS,VBSO,VLDDD,VLDSS
      write(4,77) VDSO,QGF,QGB,QD,-(QGF+QGB+QBY+QD),QBY
   77 format(6(D10.4,2x))
C
C  VBINIT is used as an initial guess for VBS in the next
C  VDSO step.
C
      VBINIT(I)=VBSS
C
  900 CONTINUE
C
C  ALL DONE
C
 9999 CONTINUE
C
      END
```

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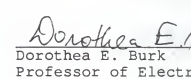

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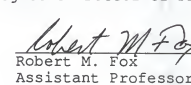

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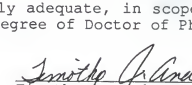

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